

p 12

A blue, horizontally-oriented oval shape with a slightly irregular, hand-drawn appearance. It contains the word "Fenlow" in a bold, black, sans-serif font.

Fenlow

DIGITAL VOLTMETER

TYPE 501 - A

MP MASTER



MA23403

DIGITAL VOLTMETER

TYPE 501-A

WITH PLUG-IN TYPE A

(D.C. VOLTAGE-MANUAL RANGING)

INSTRUCTION MANUAL

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97 —

JUNE 1969

DO NOT ADJUST ANY POTENTIOMETERS ON
THIS INSTRUMENT BEFORE REFERRING TO SECTION FIVE.

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FIG. No.

DVM type 501

General

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Grounded Power Supply

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Rear Floating Unit

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PLUG-IN type A

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1. SPECIFICATION FOR DVM TYPE 501-A

VOLTAGE RANGES

Range (1)	0 - 0.1 Volt
Range (2)	0 - 1.0 Volt
Range (3)	0 - 10 Volts
Range (4)	0 - 100 Volts
Range (5)	0 - 1000 Volts

OVERRANGING

Overranging of 40% on all ranges is provided for, with overload indicated by all decimal points being illuminated when the voltage is outside the 40% overrange.

INPUT IMPEDANCE

Range (1)	greater than	100 Megohms
Range (2)	" "	1000 Megohms
Range (3)	" "	10,000 Megohms
Range (4)	" "	10 Megohms
Range (5)	" "	10 Megohms

COMMON MODE RESISTANCE

Greater than 10,000 Megohms

Common mode voltage maximum 500 volts

SERIES MODE REJECTION

Rejection of interference at the mains frequency (even when this deviates from its nominal 50 Hz or 60 Hz) and harmonics;

Without the use of the filter 70 dB.

With the filter 100 dB.

Both for deviation of the mains frequency between 45 Hz and 65 Hz.

COMMON MODE REJECTION

(Ratio between the common mode voltages and the voltage read by the DVM)

At D.C. 140 dB

At mains frequency 150 dB

Both measured with 1000 ohms out of balance in either Input high or Input low.

TEMPERATURE RANGE

Ambient temperature 0 to 40 degrees centigrade, for the instrument to meet accuracy requirements.

INPUT OFFSET CURRENT

Balanced to zero by front panel controls, changes with temperature;

Range (1)	)	
Range (2)	)	10^{-11} amps. per degree centigrade
Range (3)	)	
Range (4)		10^{-12} amps. per degree centigrade
Range (5)		10^{-13} amps. per degree centigrade

SENSITIVITY

Range (1)	10 microvolts
Range (2)	100 microvolts
Range (3)	1 millivolt
Range (4)	10 millivolts
Range (5)	100 millivolts

RESOLUTION

1 part in 14,000

ACCURACY

$\pm 0.01\% \pm 1$ digit

POLARITY INDICATION

Automatic by sign indicator tube.

SAMPLING RATE

For complete numerical information and sign;

Internal:

25 samples per second.

External:

Up to a maximum of 25 samples per second as demanded by interrogate pulse. Complete sign determination is carried out within the 40 milliseconds (the measurement is made during the mains period succeeding the interrogate pulse).

NOTE. When operated on 60 Hz mains frequency the maximum rate is 30.

DISPLAY

By NIXIE indicator tubes with storage to give anti-blink readout. Maximum reading + 1400.0.

CALIBRATION

By means of a Muirhead reference cell. Temperature coefficient 5 microvolts per degree centigrade.

DATA INPUTS AND OUTPUTS

'0' state is less than + 0.5 volts at a maximum of 5 milliamps.

'1' state is between + 3.0 volts and + 5.0 volts at a maximum of 3 milliamps.

The Grounded Logic Common which is taken to the rear connector is not earthed inside the instrument. This enables the common to be earthed when used on printers etc., thus avoiding earth loops.

CALIBRATION AND ZERO BALANCE

Provision is made for calibration and zero adjustment by means of screwdriver adjusted potentiometers on the front panel. For zero balance provision has been made for both voltage and current balance.

ADDITIONAL RANGE

For non-logging applications an approximate X5 facility on the 0.1 volt range is provided.

2. OPERATING INSTRUCTIONS

2.1 MOUNTING

For normal bench use the carrying handle can be used to raise the front of the instrument for a better viewing angle. To mount the instrument in a standard rack the two bosses are removed by taking out six screws and are replaced by rack mounting side cheeks, Fenlow Part No. P1455.

2.2 MAINS VOLTAGE

Provision is made for setting the instrument to either 230 volts or 115 volts. On the 230 volt tapping the instrument will work from 200 to 255 volts and on the 115 volt tapping the instrument will work from 100 to 130 volts, and the frequency range may be from 45 Hz to 65 Hz. The tapping adjustment is carried out after removal of the top cover, which is removed by sliding back after releasing the Dzus fastener at the rear.

2.3 INPUT CONNECTOR

The input is connected by means of a three-way screened connector. The three connections are - Input high, Input low and Guard, the main body of the connector is connected to an outer screen and the instrument chassis. The connections are as shown in Fig. 1.

The Guard connection must be connected to either of the Input low, Input high or source of common mode, in the absence of common mode voltages or when the common mode voltage is between Input low and mains earth, the Guard and Input low should be

connected together externally.

No damage will be caused if the Guard is left free but errors can occur in certain circumstances on the most sensitive range.

2.4 REAR CONNECTOR

The output connector is a multiway socket, the connections are as shown in Fig.1.

2.5 FRONT PANEL CONTROLS

Either the interrogate internal or the interrogate external control must be pressed to operate the instrument, on internal the instrument is self triggered, on external it can be inhibited by means of the rear connector.

For most applications the Input filter is not necessary but in very noisy environments it can be used to reduce the interference. On the 100 volt and 1,000 volt ranges the filter time constant is determined by the attenuator resistors and is 1 second on the 100 volt range and 0.1 seconds on the 1,000 volt range. On the lower ranges the time constant is 0.01 seconds for zero source resistance, but this filtering may be increased by using an appropriate series resistance (the internal capacity is 1 microfarad) when the filter is switched in.

The voltage range is selected by the front panel switches (for the X5 facility both the 0.1 volt and 1.0 volt buttons must be pressed and the reading must then be divided by five). The instrument will recover within 2 milliseconds from a severe overload of up to 3 milliamps driven into the input terminals (the overload input resistance is approximately 10 Kohms).

Calibration of the instrument can be made by pressing one of the calibration check buttons, and adjusting the calibration potentiometer until the reading displayed is 10,000. Provision is made for adjusting separately the voltage and current zeros. The current and voltage balance controls should be adjusted so that a change of source resistance does not shift the zero. If the source impedance is changed from zero to 1 Megohm, a current of 0.1 nano-amperes will give rise to 100 microvolts, which is equal to the least significant digit on the 1.0 volt range. Zero balance can be carried out by switching to this range and setting the voltage adjustment to give zero when the input terminals are shorted together, and the current adjustment to give zero when 1 Megohm is used as a source, repeating this procedure until zero is obtained for both conditions. For many uses the exact current zero is not important and the zero can be set by using only the voltage control, pressing the zero button and selecting the 0.1 volt range.

2.6 SYSTEMS USE

For systems use i.e. in data loggers or when used with printers and punches, various waveforms have been brought to the rear connector and various inputs can be applied. Fig.1 shows the pin connections.

They are:

1. All the Decimal Outputs, coded in BCD 8421 code.

2. Sign information, positive indicated by a '1' state negative indicated by a '0' state.

3. Decimal Points, 5 wire system, range selected indicated by a '1' state.

4. Overload, '1' state for overload.

5. Master Gating Output ($\bar{G}$) (square wave at half the mains frequency).

6. Interrogate Input, which for no interrogation is held at a '0', for interrogation a positive pulse of length at least 50 microseconds is required. When switched to internal the external interrogation has no effect.

7. Analogue Complete Pulse, this is a 4 millisecond positive pulse that occurs when the analogue input data is finished with.

8. Instruction to Print, a positive pulse of 4 milliseconds on internal, 4 milliseconds plus $2n$ mains periods as determined by the interrogation rate on external.

9. Mains Schmitt Trigger Overriding Input. For normal use this terminal MUST be left open circuit. To override the internal Schmitt drive the externally applied waveform must be a square wave with levels between (0 to + 0.3) volts and (+ 3.0 to 5.0) volts, from a source impedance less than 300 ohms.

10. With auto and command ranging plug-in units, three inputs are provided for the command ranging, these are coded in a 421 code.

11. With the linearisation plug-in unit, two inputs are provided for.

12. A version of the voltmeter 501/MB has the input connector at the rear.

13. With the A.C./D.C. converter plug-in unit, the A.C. symbol drive is provided for.

14. + 5 volts at 100 milliamps is provided for external use if required.

2.7 MASTER SLAVE OPERATION

It is sometimes convenient in fast logging systems to use several Digital Voltmeters working in parallel, and it is important that the readings taken by different Digital Voltmeters should be either simultaneous or alternating. Two voltmeters not interconnected can take up either of the two modes according to the starting condition. To determine one mode or the other without ambiguity, provision has been made for operating the voltmeters in a master slave fashion. For simultaneous operation:

The Master Gating Output (G) of the two Digital Voltmeters have to be connected to an external Equivalence Gate, the output of which is used as the Schmitt overriding waveform of the slave Digital Voltmeter (see page 6).

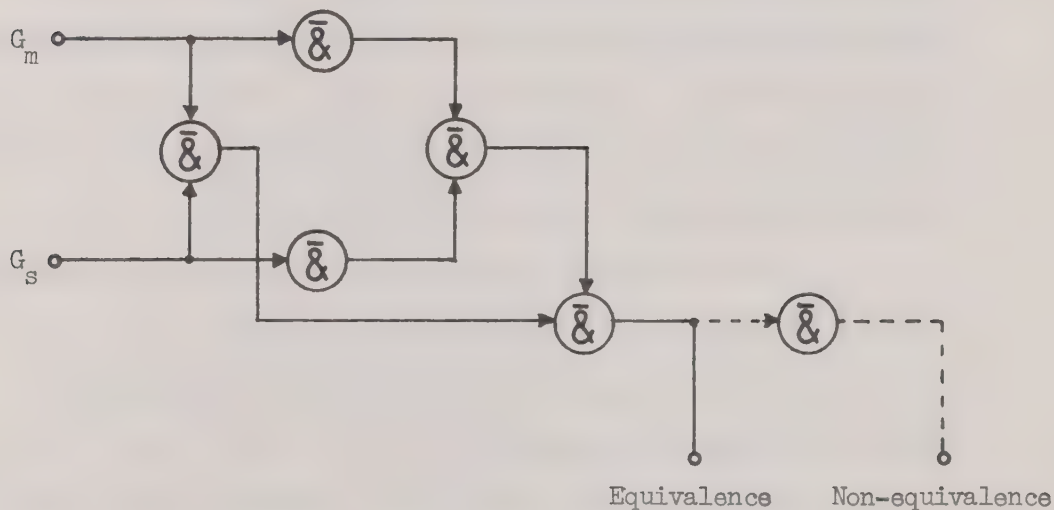
For alternating operation the procedure is the same as above but a Non-equivalence Gate is used (see page 6).

2.8 NON-SYNCHRONOUS WORKING

The overriding Schmitt Trigger terminal may be used to

obtain the very high rejection of series mode interference at frequencies not equal to the mains frequency, by driving the overriding terminal from the signal for which rejection is required. (It will have to be provided as a square wave). The range covered is from 45 Hz to 65 Hz, but some internal adjustment of the trimmers on the centre strobe and offsets will have to be made.

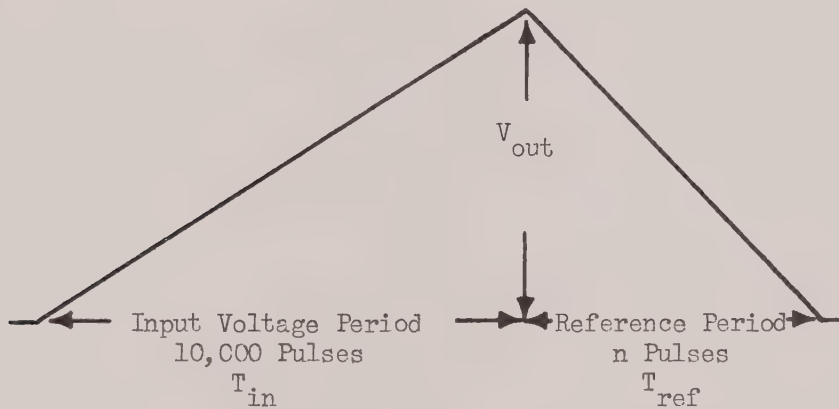
A typical Equivalence (Non-equivalence) Gate using NAND gates only :



3. SYSTEM DESCRIPTION

3.1 GENERAL

The Integrating Digital Voltmeter type 501 measures the applied input voltage by applying it to an integrator for a fixed period of time. The time taken to return the integrator to zero when a reference voltage of opposite polarity is applied is used as an analogue of the input voltage.



BASIC TIMING WAVEFORM DIAGRAM

A simplified block schematic diagram to illustrate the function of the system is shown in Fig. 2.

The input voltage is applied to the integrator until a counter has counted 10,000 pulses. The output of the integrator is then returned to zero by applying a reference voltage of opposite polarity. At the same time pulses from the same source are fed into the counter, the number of pulses (n) counted during the reference period is then displayed at the end of the reference period. With careful scaling of the reference voltage this number displayed is

that of the applied voltage. From the basic timing waveform diagram, the integrator output voltage

$$V_{out} = V_{in} \frac{T_{in}}{C.R} \text{ --- (1)}$$

where C is the feedback capacitor of the integrator and R is the input resistor. Similarly

$$V_{out} = V_{ref} \frac{T_{ref}}{C.R} \text{ --- (2)}$$

Equating (1) and (2)

$$V_{in} = V_{ref} \frac{T_{ref}}{T_{in}} \text{ --- (3)}$$

Now T_{in} is the time required for the counter to count 10,000 pulses therefore

$$T_{in} = \frac{10,000}{f} \text{ --- (4)}$$

where f is the frequency of the oscillator.

$$\text{Similarly } T_{ref} = \frac{n}{f} \text{ --- (5)}$$

From (3), (4) and (5)

$$V_{in} = V_{ref} \frac{n}{10,000}$$

$$\text{or } n = 10,000 \frac{V_{in}}{V_{ref}} \text{ --- (6)}$$

It can be seen from equation (6) that 'n' is independent of oscillator frequency and the value of C and R, provided none of these three variables change during one complete measuring interval.

With many Digital Voltmeters the period of integration of the input voltage is fixed to be equal to approximately one period of

the mains frequency, with a view to eliminating errors due to contamination of the input signal by the mains frequency and harmonics of it. With instruments which have fixed integration times, errors arise when the mains frequency changes from its normal 50 Hz or 60 Hz, and these errors can be very large. For example, if the interfering signal has a peak amplitude equal to say 10 times the D.C. voltage to be measured and the phase is in the most unfavourable condition, a 1% deviation of the mains period from the input voltage integration period will cause an error of 10% in the reading. This is clearly a great disadvantage in systems work where interfering signals are often present. Some integrating Digital Voltmeters cease to function correctly when the sign of the integration changes during the input voltage integration period. Some instruments reduce the effects of interference by the use of filters and these can be effective enough but only at the expense of sampling rate. Twin 'T' filters, etc., would need to track the mains frequency to be effective enough. Multi-section low pass filters are often used. In either case up to eight time constants may have to elapse before the input voltage has reached its final level, reducing the possible sampling rate to seconds.

In the DVM type 501 the input voltage integration period is accurately locked to the mains frequency by servo controlling the oscillator using the counter and an auxiliary early and late strobe control loop. The above is possible as the measurement is independent of oscillator frequency. The system design is such that a reversal of sign of the integrator output during the input voltage

integration period does not affect the system. The gain of the oscillator servo control loop ensures that the difference between the input voltage integration period and the mains period is reduced by a factor of 100, i.e. 1% difference is reduced to 0.01% difference and the errors due to interference are reduced accordingly compared with fixed period integration systems.

Parts of the DVM are floating and screened to facilitate differential operation in the presence of common mode voltages. Connections to and from the floating and grounded units are made via pulse transformers.

3.2 INPUT AMPLIFIER AND ATTENUATOR SYSTEM

The purpose of the input amplifier is to provide:

- a) scaling of the input voltages to a suitable level for integration;
- b) high input impedance. This ensures that there is no loading effect when the input terminals of the DVM are connected to the applied voltage, which can have a fairly high internal resistance;
- c) low output impedance and thus eliminating the loading effect of the input resistor of the integrator;
- d) high static gain. This is necessary to give high accuracy;
- e) high dynamic gain for accuracy when the instrument is used for logging at high speeds.

Figure 3 shows the arrangement of the input amplifier and attenuator system. On the 100 volt and 1,000 volt ranges the input voltage is attenuated using the precision resistors R_1 and R_2 . On

the 0.1 volt, 1.0 volt and 10 volt ranges the gain of the input amplifier is set by R_3 and R_4 .

3.3 REFERENCE VOLTAGE AND REFERENCE AMPLIFIER

The reference voltage is that of a Muirhead unsaturated reference cell.

The purpose of the reference amplifier is to give:

- a) high input impedance. This ensures that there is no loading effect on the reference cell;
- b) low output impedance and thus eliminating the loading effect of the input resistor of the integrator;
- c) high static gain. This is necessary to give high accuracy;
- d) high dynamic gain for accuracy when the sign of the reference voltage changes.

The gain of the reference amplifier is set by two resistors similar to the gain setting method of the input amplifier on the 0.1 volt and 1.0 volt ranges using R_3 and R_4 .

3.4 INTEGRATOR

The integrator consists of an amplifier, feedback capacitor and an input resistor.

For the slope of the integrator output (when an input signal is applied) to be linear, the amplifier will have to have:

- a) high dynamic gain;
- b) low output impedance. This ensures that the zero detector input does not load the output of the integrator.

3.5 ZERO DETECTOR

The purpose of the zero detector is to give:

a) a zero detector pulse, this is a pulse for determining the end of the reference period and occurs when the integrator output reaches its initial state (approximately zero);

b) sign dependent levels, this is used to determine the sign of the reference voltage that will be applied during the reference period.

3.6 FLOATING LOGIC

The purpose of the floating logic is for controlling the input and reference relay. Pulses for the start and stop of the input voltage integration period and start of the reference period are fed from the grounded logic via a pulse transformer. The end of the reference period is determined by a pulse from the zero detector.

3.7 GROUNDED LOGIC

The grounded logic consist of the:

a) oscillator servo control loop, this is for controlling the oscillator so that it tracks the mains frequency;

b) interrogation unit, this unit can be interrogated internally or externally. The unit provides a pulse for transferring the data on the counters at the end of the reference period to the store. When a complete input voltage integration period succeeding the interrogate pulse occurs, a transfer to store pulse occurs at the end of the reference period for the above input voltage integration period. This unit also provides outputs for use with data loggers, printers, etc.

c) logic for controlling the oscillator pulses into the counters and pulses for controlling the floating logic via a pulse

transformer.

3.8 COUNTERS, STORE AND READOUT.

The counters count in B.C.D. 8421 code with the storage in the same code which provides outputs for printers etc. The decimal drive to the NIXIE tubes is obtained by decoding the outputs of the storage.

The whole counter consists of 4 decades plus an over-ranging bistable. Associated with the counter is a sign bistable together with its sign store and sign tube driver.

3.9 GROUNDED AND FLOATING POWER SUPPLIES

As parts of the instrument are floating two power supplies are required. The floating power supply transformer has separate primary and secondary screens and the insulation resistance between the primary and secondary windings and screens is very high to give good common mode rejection.

3.10 GENERAL EXPLANATION OF THE CONTROL OF THE COUNTERS AND INTEGRATOR

The first operation carried out during the measuring cycle is to transfer the data from the previous measurement from the counter to the store (see Fig. 4). 200 microseconds after this the counters are reset to 09900. 4 milliseconds after the previous data was transferred to the store, the input voltage is applied to the integrator by the input and reference relay and switches (Fig. 5). Simultaneously with this, pulses from the oscillator are fed via a divide by three unit into the counter. When 10,000 pulses have been counted i.e. when the reading is 19900, the voltage is removed from the integrator, leaving a voltage stored on the integrator

capacity^{of} which is proportional to the input voltage and the period for which it was applied.

At the end of the input signal period, the sign of the input voltage is determined by the state of the zero detector, and is used to determine subsequently the sign of the reference voltage necessary to bring the output of the integrator to zero. However, before applying the reference voltage to the integrator, two extra periods are used. Immediately after the integration of the input voltage an offset voltage is applied (positive for a previously positive input voltage and negative for a previously negative input voltage). This is done for two reasons. Firstly to eliminate the effects of a finite rise time on application of the reference, which would give rise to nonlinearity around zero, and secondly to give independent adjustment of the zero for either sign. It also obviates difficulties due to delays in the counters and prevents the production of spurious zero crossing pulses. The second period after the sign determination (approximately 4 milliseconds) is to allow the relays which switch from input signal to reference and the sign of the reference to settle down. During this period no input is applied to the integrator and no pulses are applied to the counters. Pulses are applied to the counter at a frequency of approximately 500 KHz both during the input signal period and the offset period. The end of the offset period is determined when the counter reaches 19980 making the offset period approximately 160 microseconds.

The start of the reference period is determined by the return of a monostable which gives the 4 milliseconds delay from

approximately the end of the input signal period. During the reference period, pulses from the oscillator (at approximately 1.5 MHz) are fed directly into the counter unit until the output of the integrator reaches its initial state (approximately zero), when a pulse (which will be subsequently referred to as the 'F' pulse) from the zero detector switches off the reference voltage and the pulses from the oscillator to the counter. This data is transferred to the store at the start of the next measurement interval.

4. TECHNICAL DESCRIPTION

4.1 LOGIC SYMBOLOGY

The positive logic convention is used.

AND gate



Truth table

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

OR gate



Truth table

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

NAND gate



Truth table

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

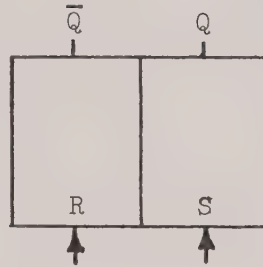
NOR gate



Truth table

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

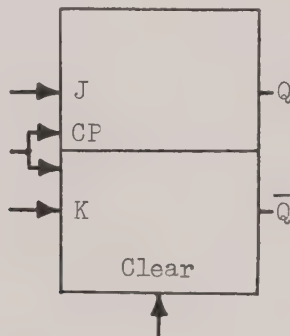
R.S. bistable



A negative pulse (transition from a 1 to a 0 state) at S sets the bistable i.e. $Q = 1$ and $\bar{Q} = 0$.

A negative pulse at R resets the bistable i.e. $Q = 0$.

J.K. bistable



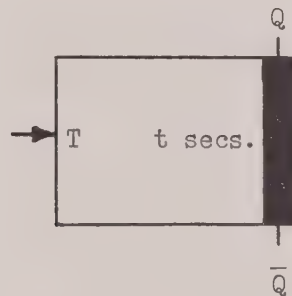
Steering table

From	To	Require	
		J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

where 'X' indicates a "don't care" state i.e. it can be a 1 or a 0.

The bistable can be cleared i.e. $Q = 0$, if the clear terminal is taken to a 0 state.

Monostable



Normally the monostable is in the reset state i.e. $Q = 0$. When a negative pulse is applied at T, the monostable is set i.e. $Q = 1$ for a duration determined by a CR time constant. The duration is shown in the logic box.

4.2 STANDARD INPUT AMPLIFIER AND ATTENUATOR SYSTEM

Figure 3 shows the arrangement of the input amplifier and attenuator system.

On the 100 volt and 1000 volt ranges the input is attenuated using precision resistors, on the 1000 volt range R_1 is 11 megohms and R_2 is 111.111 Kohms, on the 100 volt range R_1 is 10 megohms and R_2 is 1.11111 megohms. The values of the resistors are accurate to 0.1% with an accuracy of the ratios to 0.005% and a temperature coefficient of the matching to less than 5 parts per million per degree centigrade.

On the 10 volt range $R_3 = 0$ and $R_4 = \text{infinity}$, on the 1.0 volt range the ratio of R_3 plus R_4 to R_4 is equal to 10 and on the 0.1 volt range this ratio is 100. The values of the resistors are accurate to 0.1% with an accuracy of the ratios to 0.005% with a temperature coefficient of the matching to less than 5 parts per million per degree centigrade.

The amplifier used is a chopper stabilised operational amplifier using an F.E.T. chopper with the following specification:

D.C. gain:	2×10^7
A.C. gain:	10^5 at 1 KHz
Zero stability:	0.5 microvolts per degree centigrade
Output current:	± 5 milliamps
Output voltage:	± 15 volts

Referring to the circuit diagram (Fig.19) it can be seen that the amplifier is divided into two sections. The upper section is the main part of the amplifier which is a.c. coupled to the input terminal. D.C. and low frequency components are filtered off through the lower section which is a chopper amplifier. The combined frequency response gives a maximum gain at d.c. of 2×10^7 falling to 10^5 in a flat mid-band region extending from 10 Hz to 1 KHz.

Above 1 KHz the gain falls off at about 9 dB per octave.

The chopper is a field effect transistor. After amplification the chopped signal is demodulated. This is followed by filter circuits which remove the chopper ripple. The chopper and demodulator are driven synchronously by the multivibrator circuit at about 1 KHz.

The high frequency and low frequency components are recombined in the input stage of the a.c. amplifier. The remaining stages provide wide-band amplification incorporating the necessary frequency shaping. The output stage is a Class A emitter follower with a constant current transistor load.

The feedback circuits of the input amplifier are shown in simplified form in Fig. 3.

It can be seen that current feedback is used to give a high input impedance, the value of which is given by the relation:

$$Z_{in} = \frac{A \cdot R}{G}$$

where: A is the open loop gain.

R is the actual input resistance of the amplifier

G is the closed loop gain.

4.2 COUNTER, STORE AND READOUT SYSTEM

Integrated circuit counter, storage and decoder NIXIE driver units are used, as shown in Fig. 14.

The counters count in B.C.D. 8421 code with the storage also in B.C.D. which provides outputs for printers etc. The decimal drive to the NIXIE tubes is obtained by decoding the outputs of the storage I.C's.

The whole counter consists of 4 decades plus an Overranging Bistable (H). Associated with the counter is a Sign Bistable (I) together with its sign store and sign tube driver.

The transfer to store operation which is the first part of the measuring cycle, is carried out by applying a positive pulse of 20 microseconds to the clock pulse line on each of the storage units, the same pulse is also applied to the Overranging and Sign storage Bistables.

After the Transfer to Store, the counters are reset by applying a positive pulse of 20 microseconds to the decade counters and a negative pulse of the same period to the Overranging and Sign Bistables. The counter is reset to - 09900.

For the control of the logical sequences, various timing edges are taken from the counter unit. They are:

- 19900 - To determine the end of the input signal period.
- 19980 - To determine the end of the offset period.
- 19890 - For the start of the centre strobe monostable
(The purpose of this will be explained later).
- 14000 - Overload indication and for use on autoranging
plug-in units.
- 00999 - For use with autoranging plug-in units.

These outputs are obtained by decoding the outputs of the appropriate counters and are shown on Fig. 14.

The decimal point indicators are operated by the appropriate voltage range switch. Overload indication is shown by displaying all the decimal points by means of the Overload Bistable (C) which is

triggered by the 14000 reading.

The sign tube also has the symbol A.C. as an electrode. Provision is made for the illumination of this when an A.C. plug-in unit is being used.

4.4 OSCILLATOR CONTROL LOOP

The control of the input voltage integration period to be equal to one mains period is carried out by an early and late strobe control loop.

Diagrams showing the oscillator control loop timing waveforms and the block schematic are given in Figs. 6 and 7 respectively. The oscillator is a self starting multivibrator formed by integrated circuit NAND gates, and is supplied from very stable and ripple free power lines. The multivibrator is voltage controlled in frequency. The frequency is controlled so that 30,000 pulses correspond to one mains period to within 2 microseconds on average. This control is carried out by using an error signal which is derived from overlapping strobe gates which are fed via a shaped amplifier to the oscillator voltage control line. To facilitate the correct control of the oscillator error signals are derived from two gates, the early and late strobe gates, both supplied on one input from the centre strobe and on the other input by the early and late strobe respectively. The centre strobe is derived from an adjustable monostable which is triggered from the counter and is hence timed by the oscillator frequency. The early and late strobe pulses are derived from a monostable timed from the Mains Schmitt Trigger and therefore shift in time as the mains period alters. The gain of the oscillator control

loop is determined by the outputs from the strobe gates and the amplifier, and has been arranged to reduce the effect of mains variation on series mode errors by a factor of about 100 times.

It is important to note that because of the long smoothing time in the amplifier shaping, no errors are caused by misfiring of the Mains Schmitt Trigger due to distortion of the mains waveform near zero. It is also important to note that the system accuracy does not depend upon this control loop, it is only introduced to remove the effects of spurious series mode signals.

4.5 LOGICAL SYSTEM

This description should be read in conjunction with the main timing waveform diagram Fig. 8 and the block schematic diagram Fig. 10. Figure 10 is a complete system diagram showing all the logical units. The parts of the unit which are floating are shown on the left hand side enclosed by the dotted lines, all the couplings to this unit being made by transformers.

As mentioned previously the system is worked synchronously with the mains frequency, the initiation of the measuring cycle being determined by a Schmitt Trigger circuit working from the mains waveform (1), and provides an output square wave, waveform (2). Before the integration period commences the data in the Counter is transferred to the store, and the Counter is reset to - 09900 by waveform (B). The transference of the data to the store on internal is carried out at a rate of half the mains frequency, by a pulse which is derived indirectly from the Master Gating Bistable (G), waveform (3). On external the rate of transference of data is determined by the

interrogation rate.

A delay before resetting the Counter is provided by monostable (C), waveform (4), which has a period of 200 microseconds and is triggered directly from the Master Gating Bistable (G).

Having transferred to store and reset the Counter a further delay of 4 milliseconds is provided by the Input Start and Strobe Monostable (A), waveform (5), which is triggered from the Mains Schmitt Trigger.

The input voltage and the reference voltage are applied to the same input of the Integrator by means of a relay, but are in addition gated by transistor switches to give precise timing. It is convenient to proceed by explaining the operation of this relay, so that it will be understood that it is in its correct state when we explain the gating of the transistor switches, which pass the input voltage or reference voltage to the Integrator.

The Input and Reference Relay is operated via a buffer from the Input and Reference Relay Bistable (M), waveform (24). It is set indirectly when the Counter reaches 19980 (via the Floating Logic Control Pulse Mixer and the Offset Bistable). The relay is then in the reference voltage position. It is reset indirectly by the Master Gating Bistable (via the 'Artificial F' Pulse Transformer). The relay is now in the input voltage position. The timing of the relay allows about 4 milliseconds before the voltages are used, allowing for the relay bounce etc., to disappear.

After the trailing edge of the Input Start and Strobe Monostable (A) which is triggered from the Mains Schmitt Trigger, and when the Master Gating Bistable is in the set state, the first oscillator (divided by three) pulse triggers the 500 KHz Pulse Gating Bistable (A), waveform (15). This allows pulses from the Divide by Three Unit to pass into the Counter. Also on the leading edge of bistable (A), the Input and Reference Bistable (K), waveform (22), is set, via the Floating Logic Control Pulse Mixer. This bistable initiates the integration of the input voltage.

The next operation is when 10,000 pulses have passed into the Counter i.e. when the Counter reads 19900. At this point a pulse, waveform (12), to determine the end of the input voltage integration period occurs. This pulse resets the Input and Reference Bistable and sets the Offset Bistable (L), waveform (23), via the Floating Logic Control Pulse Mixer. Thus the input voltage is removed from the Integrator and according to the sign of the output of the Zero Detector Comparator, either the Positive or Negative Offset Gate is opened putting an offset voltage on to the input of the Integrator. The polarity of this voltage is determined by the state of the Sign Relay Bistable (N), waveform (25). At the beginning of the offset period the inhibit on the Sign Relay Bistable is removed for about 5 microseconds, thus allowing this bistable to set its state according to the polarity of the output of Zero Detector Comparator. This bistable then cannot change its state until the same point of the next cycle irrespective of the polarity of the output of the Zero Detector Comparator.

The offset voltage is applied for 80 pulses i.e. until the Counter reaches 19980, at which time a pulse, waveform (11), to determine the end of the offset period resets the 500 KHz Pulse Gating Bistable, thus removing the pulses from the Counter. This pulse also resets the Offset Bistable, via the Floating Logic Control Pulse Mixer.

The three following bistables:

Input and Reference (K);

Offset (L);

Input and Reference Relay (M);

are concerned with the switching of the input, offset and reference voltages. They are set and reset by pulses from the Floating Logic Control Pulse Former, 'F' and 'Artificial F' Pulse Mixer and they are intercoupled to follow the sequence shown on Fig. 8. The trailing edge of the Offset Bistable sets the Input and Reference Relay Bistable (M), waveform (24), which via the buffer changes the relay over to the reference position.

Because the Input Start and Strobe Monostable (A), waveform (5), is triggered from the Mains Schmitt Trigger it has been retriggered and its trailing edge (which lies almost at the same time as the end of the input voltage integration period) is used to trigger, on alternate cycles as determined by the Master Gating Bistable being in the reset state, a further monostable of length 4 milliseconds, the Reference Start Monostable (B), waveform (6). The trailing edge of the Reference Start Monostable triggers the 1.5 MHz Pulse Gating Bistable (B), waveform (16), on the next

oscillator pulse, which allows pulses into the Counter. This bistable also sets the Input and Reference Bistable, via the Floating Logic Control Pulse Mixer, thus switching the reference voltage into the Integrator. The sign of the applied reference is determined by the state of the Sign Relay via the buffer and Sign Relay Bistable.

The voltage on the output of the Integrator is now moving linearly towards zero. When it passes the point where the Zero Detector Comparator changes state (this level also corresponds to the Integrator starting level and therefore it need not be exactly zero) it produces an 'F' pulse from the 'F' Pulse Former, waveform (18). This pulse resets the Input and Reference Bistable, via the 'F' and 'Artificial F' Pulse Mixer thus removing the reference voltage from the Integrator. This pulse also resets the 1.5 MHz Pulse Gating Bistable, via the Positive Sign and 'F' Pulse Mixer and Separator thus removing the pulses from the Counter. At the next transition of the Master Gating Bistable, a pulse which is also used as the 'Artificial F' pulse resets the Input and Reference Relay Bistable via the 'F' and 'Artificial F' Pulse Mixer. At this time the data is available to be transferred to the store either by internal or external interrogation.

The Sign Bistable (I), waveform (26), is set (i.e. the bistable is in the positive state) by a pulse at the time the Offset Bistable is reset. This pulse is fed from the Positive Sign Pulse Former, waveform (21), via the Positive Sign and 'F' Pulse Separator, if the Sign Relay Bistable is in the set state.

4.6 INTERROGATION SYSTEM

Figure 9 shows the timing waveforms associated with interrogation of the Digital Voltmeter. The only difference between internal and external is: on internal the Interrogate Acceptance Resettable Monostable (G) is triggered from the Reset Monostable, and the Overload Bistable (C) is reset by the leading edge of the Reference Start Monostable. On external the Interrogate Acceptance Resettable Monostable (G) is triggered from the interrogate input pulse, and the Overload Bistable (C), waveform (33) is reset by the Interrogate Pulse Store Bistable (E).

Interrogate Pulses, waveform (29), are inverted and trigger the Interrogate Acceptance Resettable Monostable (G). The normal period of this is 20 microseconds. If the interrogate pulse is too short this monostable is reset and the interrogate pulse is rejected. If the interrogate pulse is accepted, then 20 microseconds after this pulse has been applied the Interrogate Pulse Store Bistable (E), waveform (30) is set. The next time the 500 KHz Pulse Gating Bistable is set. This resets the Interrogate Pulse Store Bistable thus enabling it to accept another pulse and the Interrogate Auxiliary Store Bistable (F), waveform (31), is then set, until the Master Gating Bistable (G) is set which then resets this bistable until the next operation. Having reset the Interrogate Auxiliary Store Bistable, the Transfer to Store Monostable (E), waveform (7), is triggered which transfers the data on the Counters and sign to the Store. The trailing edge of the Transfer to Store Monostable sets the Instruction to Print Bistable (H), waveform (32), until the Interrogate Auxiliary Store Bistable

is set by a subsequent interrogation.

4.7 POWER SUPPLIES

Two power units are used in the voltmeter. One to provide the power for all the grounded circuits and the other to power the floating unit. The floating power unit is supplied from a 12 volt winding on the grounded mains transformer (T1). The supplies provided are:

Grounded power unit :-

+ 180 volts at 15 milliamps, ripple 2 volts P.P.

+ 5 volts at 1 ampere, " 50 millivolts P.P.

+ 5 volts at 50 milliamps, " 0.2 " " *

- 1.5 volts at 50 " " 0.2 " " *

* Very low ripple supplies for the oscillator and control loop amplifier.

Floating power unit :-

+ 5 volts at 150 milliamps, ripple 50 millivolts P.P.

+ 8 volts at 250 " (relay drive)

+ 36 volts at 40 " ripple 2 millivolts P.P.

- 36 volts at 40 " " 2 " "

+ 15 volts at 70 " " 1 " "

- 15 volts at 70 " " 1 " "

4.8 LOGICAL UNITS AND THEIR FUNCTION IN THE GROUNDED UNIT

Mains Schmitt Trigger.

This produces a square wave at the mains frequency which is subsequently divided by two and used to trigger some of the grounded logic. This Schmitt Trigger has an overriding separate

input taken to the rear connector to facilitate master slave operation.

Master Gating Bistable (Bistable G).

This works at half the mains frequency and is used to produce: an 'Artificial F' pulse; the gating of the Reference Start Monostable; the gating of the 500 KHz Anti pulse splitting Gate; the triggering of the Delay Reset Monostable; the separation of the early and late strobes, and the resetting of the Interrogate Auxiliary Store Bistable. It also provides an output on the rear connector.

Input Start and Strobe Monostable (Monostable A).

This is triggered at the mains frequency by the Mains Schmitt Trigger. It is used in the gating of the 500 KHz Anti pulse splitting Gate, the triggering of the Reference Start Monostable and forms the early and late strobe waveforms in conjunction with the Master Gating Bistable.

Reference Start Monostable (Monostable B).

This is triggered by the Input Start and Strobe Monostable and is gated with the Master Gating Bistable which eliminates alternate pulses. It is used to drive the Analogue Complete Pulse Buffer, to reset the Overload Bistable on internal, in gating the Positive Sign and 'F' Pulse Separator and in the 1.5 MHz Anti pulse splitting Gate.

Delay Reset Monostable (Monostable C).

This is triggered from the Master Gating Bistable and is only used to trigger the Reset Monostable.

Reset Monostable (Monostable D).

This produces the required pulse for resetting the Counters and the Sign Bistable.

Transfer to Store Monostable (Monostable E).

This is triggered from the Interrogate Auxiliary Store Bistable. It produces a suitable pulse for transferring the data on the Counters and sign to the appropriate stores. The trailing edge of this monostable triggers the Instruction to Print Bistable and it is also used in the gating of the Complement Gate.

Overload Bistable (Bistable G).

This is triggered by the 14000 pulse from the Counters and is reset by: on internal, by the Reference Start Monostable and on external, by the Interrogate Pulse Store Bistable and is used for driving the NOR gates that illuminate all the decimal points. It also provides an output on the rear connector.

1.5 MHz (NOM.) Voltage Controlled Multivibrator.

This is the oscillator which provides the pulses for the Counters. It is controlled in frequency by a voltage from the Oscillator Control Loop Error Amplifier. Its frequency is controlled to be 30,000 times the mains frequency. Associated with this oscillator are two NAND gates to make it self starting.

Divide by Three Unit.

During the input signal period the oscillator is divided by three to provide the required frequency. The higher frequency (30,000 times the mains frequency) is used during the reference period and has been chosen to shorten the reference period and

give higher working speeds.

Centre Strobe Monostable (Monostable F).

This is triggered from the Counter via the 19890 Pulse Gate and the period is adjusted to be about 40 microseconds. It is used to form the centre strobe in the Oscillator Control Loop Early and Late Strobe Gates.

500 KHz Pulse Gating Bistable (Bistable A).

This is set by the 500 KHz Anti pulse splitting Gate and is reset when the Counter reaches 19980. It is used to gate the 500 KHz pulses into the Counter, and indirectly to gate the input and offset voltage into the Integrator.

1.5 MHz Pulse Gating Bistable (Bistable B).

This is set by the 1.5 MHz Anti pulse splitting Gate and is reset by the grounded 'F' pulse or the 'artificial F' pulse via the 'F' Pulse Mixer. It is used to gate the 1.5 MHz pulses into the Counter, and indirectly to gate the reference voltage into the Integrator.

Oscillator Control Loop Error Amplifier.

This amplifier, which works from specially smoothed supply lines, is used to amplify and smooth the output from the Early and Late Strobe Gates. The output of the amplifier controls the oscillator frequency.

Late Strobe Gate.

This is driven by the Centre Strobe Monostable, Input Start and Strobe Monostable and the Master Gating Bistable. Its output provides the positive error into the Oscillator Control

Loop Error Amplifier.

Early Strobe Gate.

This is driven by the Centre Strobe Monostable and the inverse of the late strobe. Its output provides the negative error into the Oscillator Control Loop Error Amplifier.

Complement Gate.

This gate is not normally in use. It has been included because with maladjustment of the offset controls the instrument can give very large readings near the origin, i.e. instead of 00000 the instrument might show 19999 which could produce unnecessary alarms in logging systems. The complement gate changes any reading which would have been between 19980 and 19999 to 00000, since 19XXX should never occur.

1.5 MHz Oscillator Buffer.

This is provided to reduce the loading on the Oscillator.
500 KHz Anti pulse splitting Gate.

This gate is to ensure that the integration of the input voltage is started at the beginning of an oscillator pulse.

1.5 MHz Anti pulse splitting Gate.

This gate is to ensure that the integration of the reference voltage is started at the beginning of an oscillator pulse.

500 KHz Counter Pulse Gate.

This gate allows the pulses from the Divide by Three Unit to enter the Counter during the input and offset periods.

1.5 MHz Counter Pulse Gate.

This gate allows the pulses from the 1.5 MHz Oscillator Buffer to enter the Counter during the reference period. (When the lineariser plug-in unit is used these pulses are diverted through the lineariser scaling unit before entering the Counter).

'Artificial F' Pulse Transformer.

This pulse is used to reset the Input and Reference Relay Bistable. The floating logic contains two bistables which are reset by the 'F' pulse from the Zero Detector Comparator. If there is a fault on the instrument which causes the 'F' pulse not to occur, the 'Artificial F' Pulse which is coupled by the transformer resets the two bistables and simplifies fault finding.

Floating Logic Control Pulse Mixer.

To reduce the number of coupling transformers from the grounded logic to the floating unit, the pulses from the grounded logic are mixed before being applied to the transformer. These pulses are:

- a) input voltage integrate start pulse;
- b) input voltage integrate stop pulse and start of the offset;
- c) offset stop pulse;
- d) reference voltage integrate start pulse.

Positive Sign and 'F' Pulse Separator.

Pulses being fed from the floating unit via the coupling transformer are separated by two NAND gates. These pulses are the positive sign pulse (if present) and the 'F' pulse from the Zero

Detector Comparator.

Grounded 'F' and 'Artificial F' Pulse Mixer.

This combines three possible pulses. They are:

- a) 'F' pulse in normal operation;
- b) overload, in the case of an overload or absence of an 'F' pulse when the Counter is stopped at 14000;
- c) a further pulse derived from the Master Gating Bistable included to prevent a spurious mode of operation on initial switch on, caused by the large range of mains frequency being accommodated.

Analogue Complete Pulse Buffer.

This is provided on the rear connector. The pulse is used for shifting the commutator in fast logging systems.

Interrogate AND Gate.

This combines the internal and external interrogate pulses for the interrogate unit.

Interrogate Acceptance Resettable Monostable (Monostable G).

This is included to prevent the DVM being interrogated by very narrow spikes which can be caused by interference. The minimum length of positive pulse to ensure correct interrogation is 50 microseconds. The monostable is triggered by an inverter from the Interrogate AND Gate. It is reset either by its natural time constant or by the removal of the output of the Interrogate AND Gate.

Interrogate Pulse Shaper.

This provides an output pulse to drive the Interrogate

Pulse Store Bistable which follows the reset edge of the Interrogate Acceptance Resettable Monostable.

Interrogate Pulse Store Bistable (Bistable E).

This stores the fact that the DVM has been correctly interrogated either internally or externally. The bistable is reset at the beginning of the input voltage integration period, by a pulse from the 500 KHz Pulse Gating Bistable on to the clear of the J.K. Bistable.

Interrogate Auxiliary Store (Bistable F).

This store holds the interrogate information when the Interrogate Pulse Store Bistable has been reset ready to accept another input. It is reset by a pulse from the Master Gating Bistable. The output of this triggers the Transfer to Store Monostable. The setting edge of this bistable also clears the Instruction to Print Bistable.

Instruction to Print Bistable (Bistable H).

This is set by the trailing edge of the Transfer to Store Monostable. The output of this is provided on the rear connector and gives a pulse width of 4 milliseconds or 4 milliseconds plus 2 n mains periods according to the rate of the interrogation.

4.9 LOGICAL UNITS AND THEIR FUNCTION IN THE FLOATING UNIT

Floating Logic Control Pulse Former.

This inverts and amplifies the following pulses:

- a) input voltage integrate start pulse;
- b) input voltage integrate stop pulse and start of the offset;

- c) offset stop pulse;
- d) reference voltage integrate start pulse.

These pulses drive the Input and Reference Bistable and the Offset Bistable.

Input and Reference Bistable (Bistable K).

This supplies the required waveform for the Input and Reference Switch Drive.

Offset Bistable (Bistable L).

This supplies the required waveform to drive the Positive and Negative Offset Gates.

Input and Reference Relay Bistable (Bistable M).

This provides the required waveform to the Input and Reference Relay Drive.

Sign Relay Bistable (Bistable N).

This stores the sign information and uses it to drive the Positive Sign Pulse Former, to provide the required waveform for the Sign Relay Buffer and also determines the sign of the applied offset. 'F' Pulse Former.

This gives a negative pulse for either a positive or negative transition through zero. This pulse is inhibited by the Input and Reference Relay Bistable. (To prevent spurious 'F' pulses occurring during the input and offset period).

Positive Sign Pulse Former.

This gives a negative pulse at the end of the offset period which is fed via the Positive Sign and 'F' Pulse Mixer to the grounded unit when the input signal is positive.

Positive Sign and 'F' Pulse Mixer.

To save duplication of transformers, this mixes the positive sign and 'F' pulse.

'F' and 'Artificial F' Pulse Mixer.

These pulses are mixed before being fed to clear the Input and Reference Bistable. When the Offset Bistable has not been reset by its proper pulse it is reset by these mixed pulses.

Zero Detector Pre-Amplifier.

This amplifier with a gain of 100 improves the resolution of the comparator.

Zero Detector Comparator.

This is used to provide sign dependent levels which are used in the logic.

Input and Reference Relay Drive.

This circuit provides suitable drive for the relay and is driven from the Input and Reference Relay Bistable.

Sign Relay Drive.

This circuit provides a suitable drive for the sign relay and is driven by the Sign Relay Bistable.

Input and Reference Switch Drive.

This circuit is driven from the Input and Reference Bistable and provides voltages swinging either side of zero to operate the Input and Reference Switches.

Positive and Negative Offset Gates.

These gates are driven by the Offset Bistable and the Sign Relay Bistable, and switch in either a positive or negative

offset voltage into the Integrator for approximately 160 micro-seconds, producing an offset voltage corresponding to approximately 20 digits.

Automatic Hysteresis Corrector

To avoid a hysteresis effect around zero, this circuit is used to leave the Integrator output level at the beginning of a cycle at the same voltage, irrespective of the sign of the previous input voltage. The correction is applied at the time of the transfer to store.

5. ADJUSTMENTS

CAUTION

After switching on the supplies, allow the DVM one hour to reach its operating temperature. If after one hour the instrument is not performing according to its specification only the following adjustments may be attempted.

5.1 PROCEDURE

SWITCH ON AND ALLOW THE INSTRUMENT TO REACH ITS OPERATING TEMPERATURE

Short the three input leads (High, Low and Guard) together. If the instrument fails to read zero on the following ranges, refer to the sections shown:

- a) 10 volt range - see section 5.2.
- b) 0.1, 1.0, 100 or 1000 volt range - see section 5.3.
- c) 0.02 volt range - see section 5.3f

If it is required to test the accuracy, this is done in two stages. First the Input Balance is checked to ensure that the voltage of an external cell gives the same reading when its polarity is reversed. Secondly the absolute calibration is checked by means of an external standard cell. Both these procedures are described in section 5.4.

The internal facility for Calibration check may then be adjusted so that it is thereafter available for spot checking of the instruments accuracy.

See section 5.5.

5.2 ZERO ADJUSTMENT ON THE 10 VOLT RANGE

Short together all three wires of the DVM input lead. Select the 10 volt range, select Internal Interrogate, all other push buttons on the DVM to be released. With a suitable screwdriver, unlock the Dzus fasteners at the rear of the top cover of the DVM. Slide the cover towards the rear of the instrument until it is possible to lift the cover from the DVM frame. Insert a small screwdriver through the hole labelled RV3 in the top screen of the rear floating unit, to gain access to the 10 volt range zero adjusting potentiometer. Adjust this potentiometer to make the DVM reading approach zero; the final critical adjustment must make the sign indicator tube change from + to - or vice versa. ("Randomly changing sign"). The indication on the 10 volt range should then be zero $\pm$ 1 digit.

Replace the top cover and secure the Dzus fastener.

5.3 ZERO ADJUSTMENT ON THE 0.1, 1.0, 100 and 1000 VOLT RANGE

- a) Verify that the DVM complies with section 5.2.
- b) Select 100 volt range. Open circuit the Input high lead and adjust the current potentiometer labelled I on the front panel until the DVM indicates randomly changing sign.
- c) For a fine adjustment of the current potentiometer, select the 0.1 volt range and press the Filter button. With the input lead still open circuit readjust the current potentiometer to minimise the rate of change of DVM reading with time.
- d) Short circuit all three input leads of the DVM and release the Filter button, then adjust the voltage potentiometer.

labelled V on the front panel until the DVM indicates randomly changing sign.

e) Repeat (c) and (d) alternately until correct indications are obtained for both adjustments.

f) For use on the 0.02 volt range it is permissible to readjust the Voltage Potentiometers to give randomly changing sign when the input leads are shorted together. Provided that the adjustments of (c), (d) and (e) have been carried out, only a very small readjustment, equivalent to less than 5 digits, will be required. This will have no adverse effect on the other ranges.

5.4. INPUT BALANCE AND ACCURACY

a) Verify that the DVM successfully fulfils sections 5.2 and 5.3.

A standard cell of the following specification will be required in order that the following part of the procedure may be accomplished: 1.0185 - 1.0192 volts with a temperature coefficient of not greater than 5 microvolts per degree centigrade.

b) Select the 1.0 volt range. Connect Input high to the standard cell +ve terminal and Input low to the Standard cell -ve terminal. Connect the Guard lead to Input low. DVM should indicate the cell voltage ± 5 digits and display a positive sign.

RECORD THIS READING.

c) Reverse the connections to the standard cell from the DVM input lead (Guard still connected to Input low). The DVM should indicate the cell voltage ∓ 5 digits and display a negative sign.

- d) Compare this reading with that recorded in (b), subtract the magnitude of the two readings and note the difference.
- e) By adjusting the Input Balance potentiometer on the front panel, increase or decrease as is appropriate the DVM indicated reading by half the above difference.
- f) Repeat (d) and (e) until the DVM reading of the cell voltage is the same for either sign.
- g) To obtain absolute calibration of the instrument, adjust the Cal. Scale potentiometer on the front panel until correct indication of the standard Cell voltage is reached.

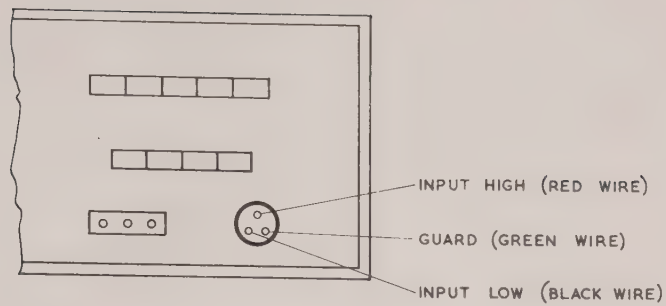
5.5 CAL. CHECK

- a) Verify that the DVM complies with Sections 5.2, 5.3 and 5.4.
- b) Remove the top cover as detailed in Section 5.2.
- c) Press the +ve Cal. Check button, note the DVM reading and use a suitable screwdriver to adjust RV4 until the DVM reads 1.0000. The potentiometer is accessible through a hole labelled RV4 in the top screen of the front floating unit.
- d) Press the -ve Cal. Check button and confirm that the -ve Cal. Check reading does not differ from the +ve Cal. Check reading by more than 1 digit.

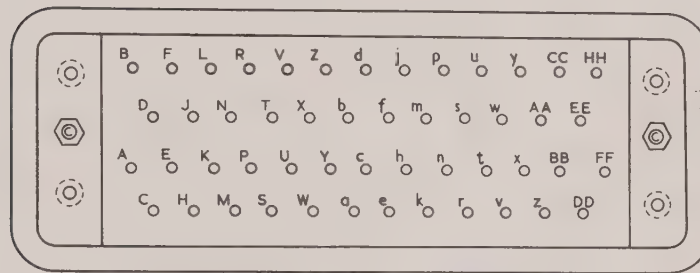
5.6 FACTORY SERVICE

If the DVM has symptoms other than these covered in this Adjustment Procedure or this procedure is not sufficiently effective in a particular case, refer to Fenlow Electronics Ltd.,

or their Agents. If standardization equipment and staff are available, a full adjustment and calibration Procedure can be obtained from Fenlow Electronics Ltd., or their Agents.



INPUT SOCKET CONNECTIONS (SKT. 2)



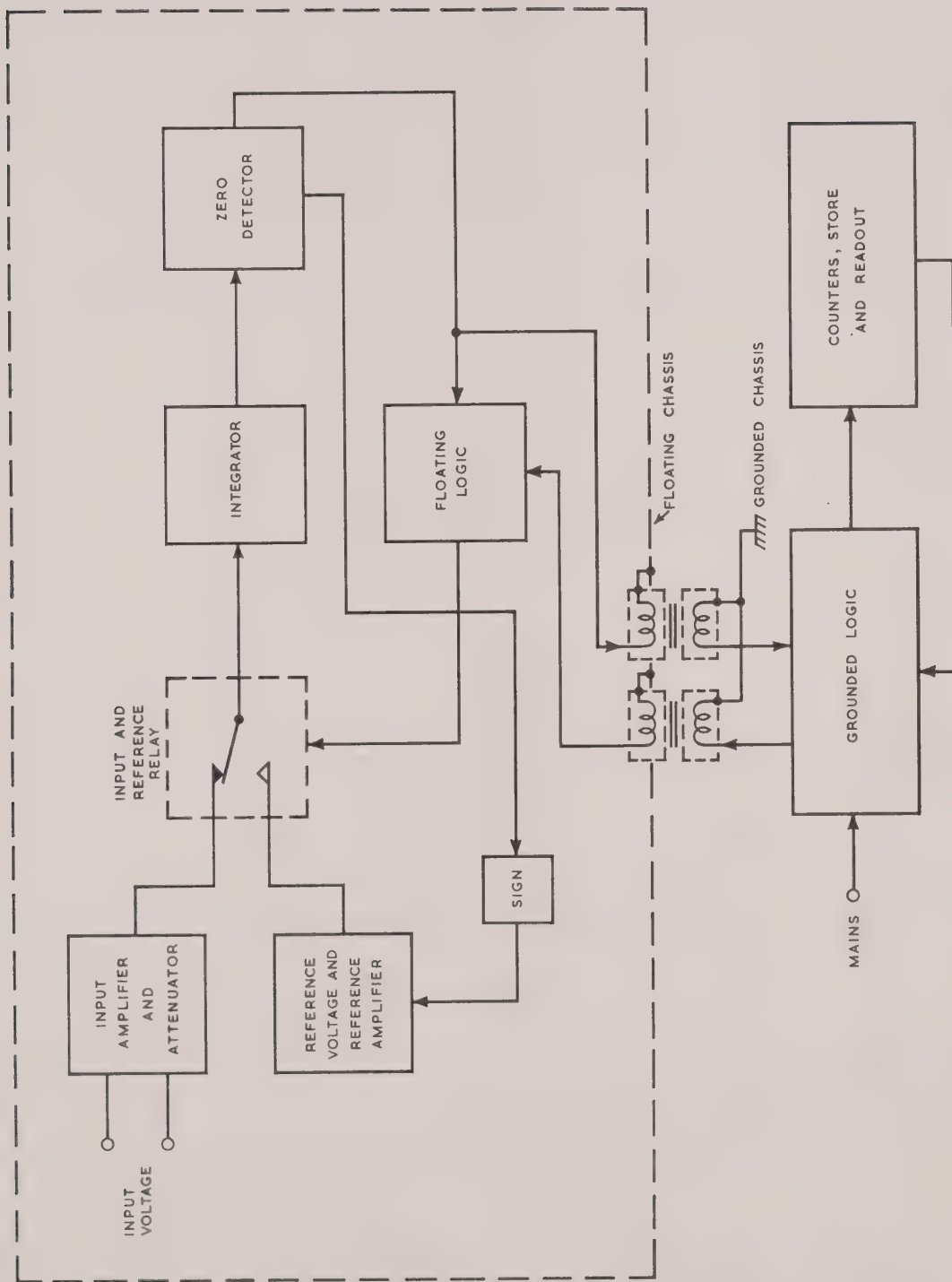
(SOCKET AS VIEWED EXTERNALLY)

FUNCTION		PIN
COUNTER A (LEAST SIGNIFICANT)	A1	A
	A2	B
	A4	C
	A8	D
COUNTER B	B1	E
	B2	F
	B4	H
	B8	J
COUNTER C	C1	K
	C2	L
	C4	M
	C8	N
COUNTER D	D1	P
	D2	R
	D4	S
	D8	T
OVERRANGING		U
SIGN		V
OVERLOAD		W

FUNCTION		PIN
VOLTAGE RANGE	0.1 VOLT	X
	1.0 VOLT	Y
	10 VOLT	Z
	100 VOLT	a
	1000 VOLT	b
MASTER GATING OUTPUT ($\bar{G}$)		c
INTERROGATE INPUT		d
ANALOGUE COMPLETE PULSE		e
INSTRUCTION TO PRINT		f
MAINS SCHMITT TRIGGER OVERRIDING INPUT		h
COMMAND RANGING PLUG-IN UNIT	A (1)	j
	B (2)	k
	C (4)	m
LINEARISER PLUG-IN UNIT	A	n
	B	p
A.C. SYMBOL / L.S. TUBE BLANKING		r
COMMON (OV)		v
+ 5 VOLTS		w

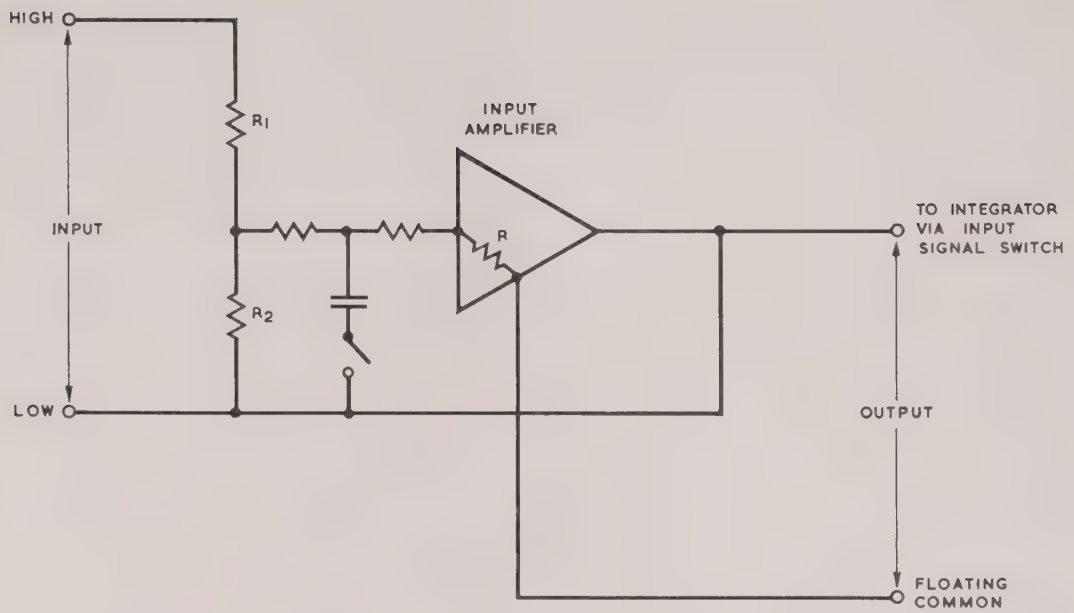
REAR SOCKET CONNECTIONS (SKT. 3)

FIGURE 1.

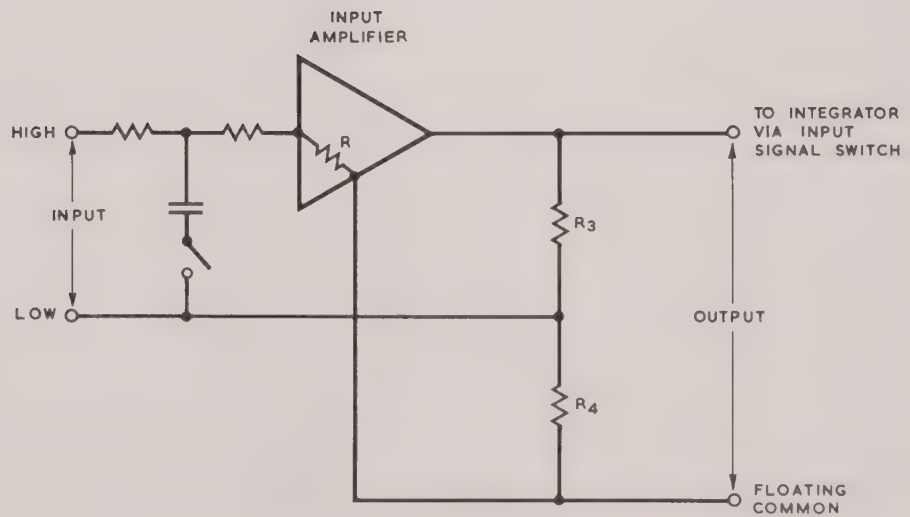


SIMPLIFIED BLOCK SCHEMATIC DIAGRAM

FIGURE 2.



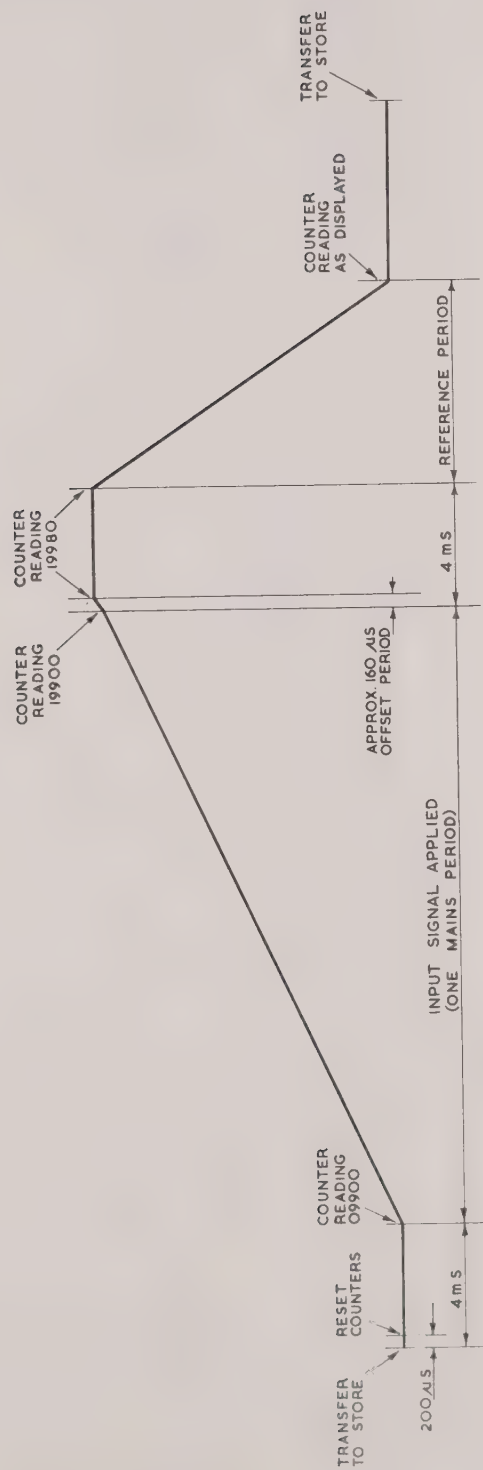
HIGH RANGES 100 V & 1000 V.



LOW RANGES 0-1V, 1-10V & 10V.

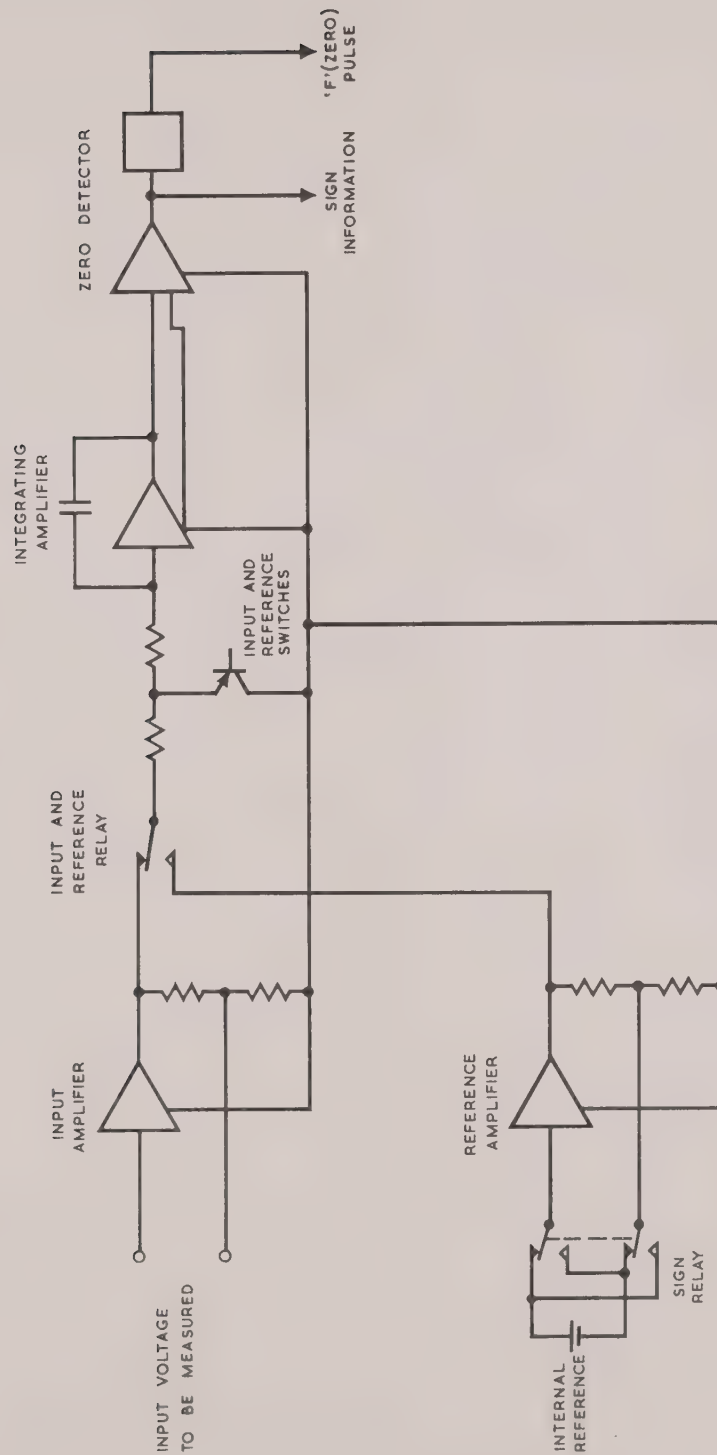
INPUT AMPLIFIER ATTENUATOR SYSTEM

FIGURE 3.



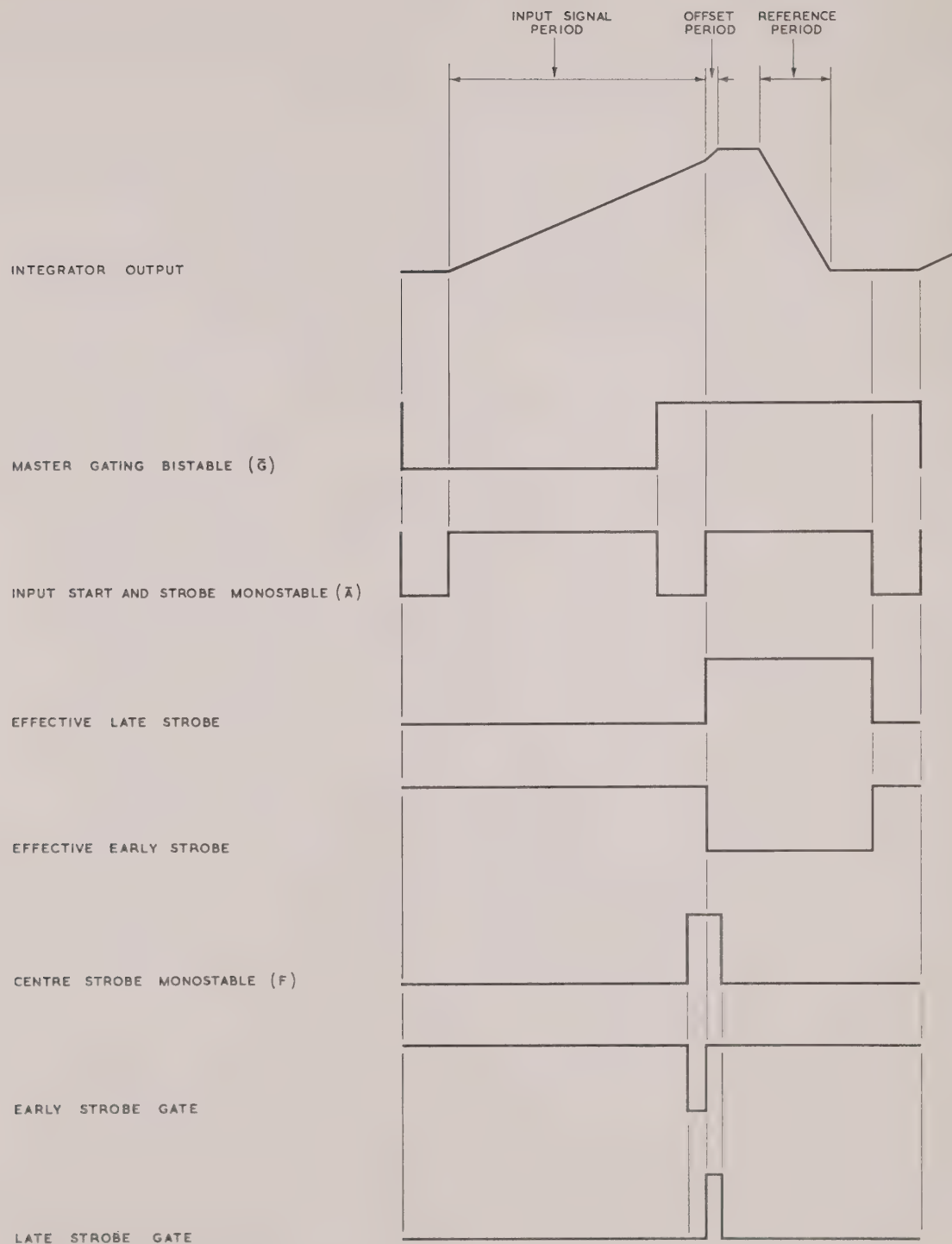
GENERAL INTEGRATOR OUTPUT TIMING WAVEFORM

FIGURE 4.

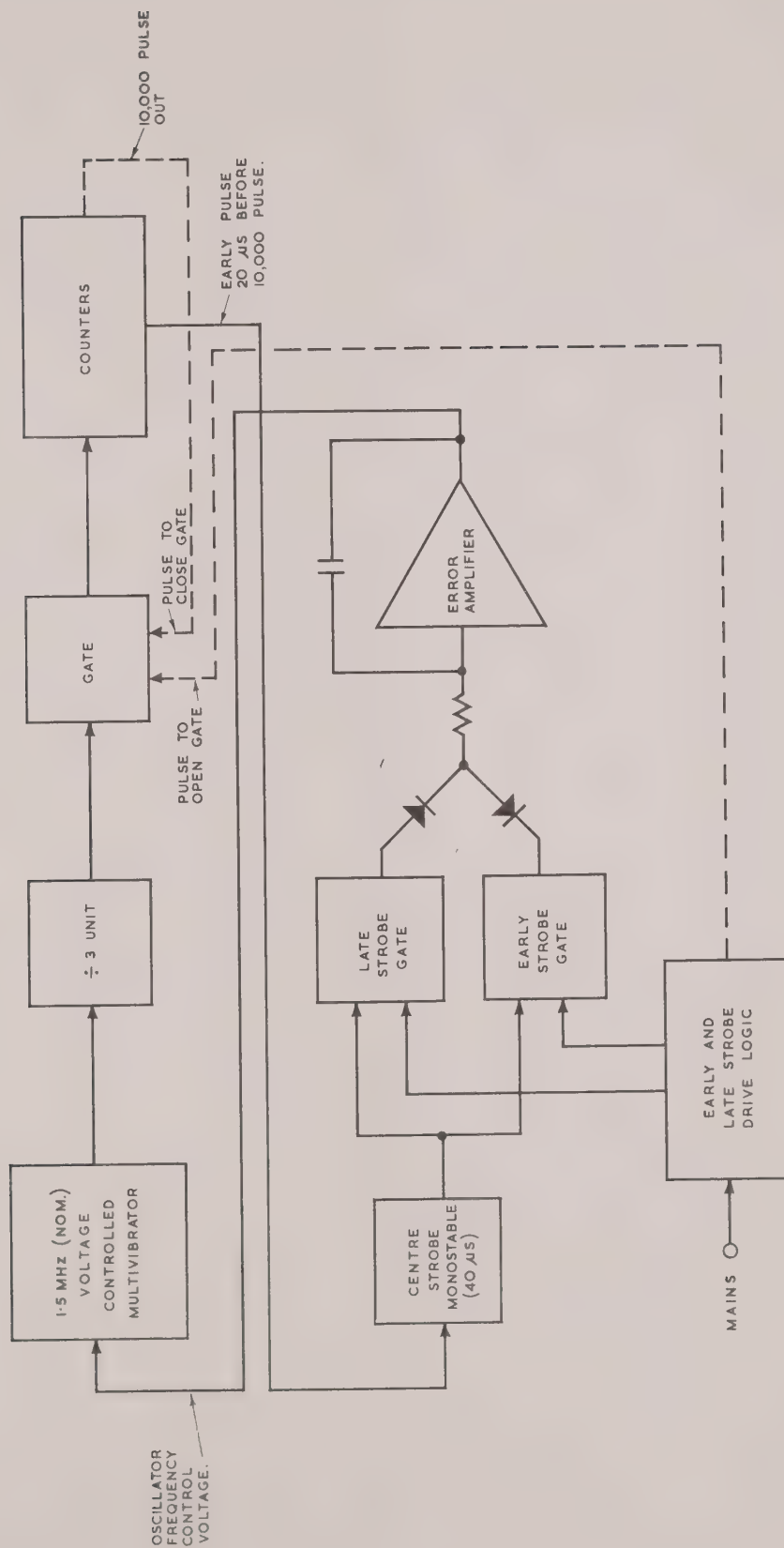


GENERAL BLOCK SCHEMATIC OF FLOATING UNIT

FIGURE 5.

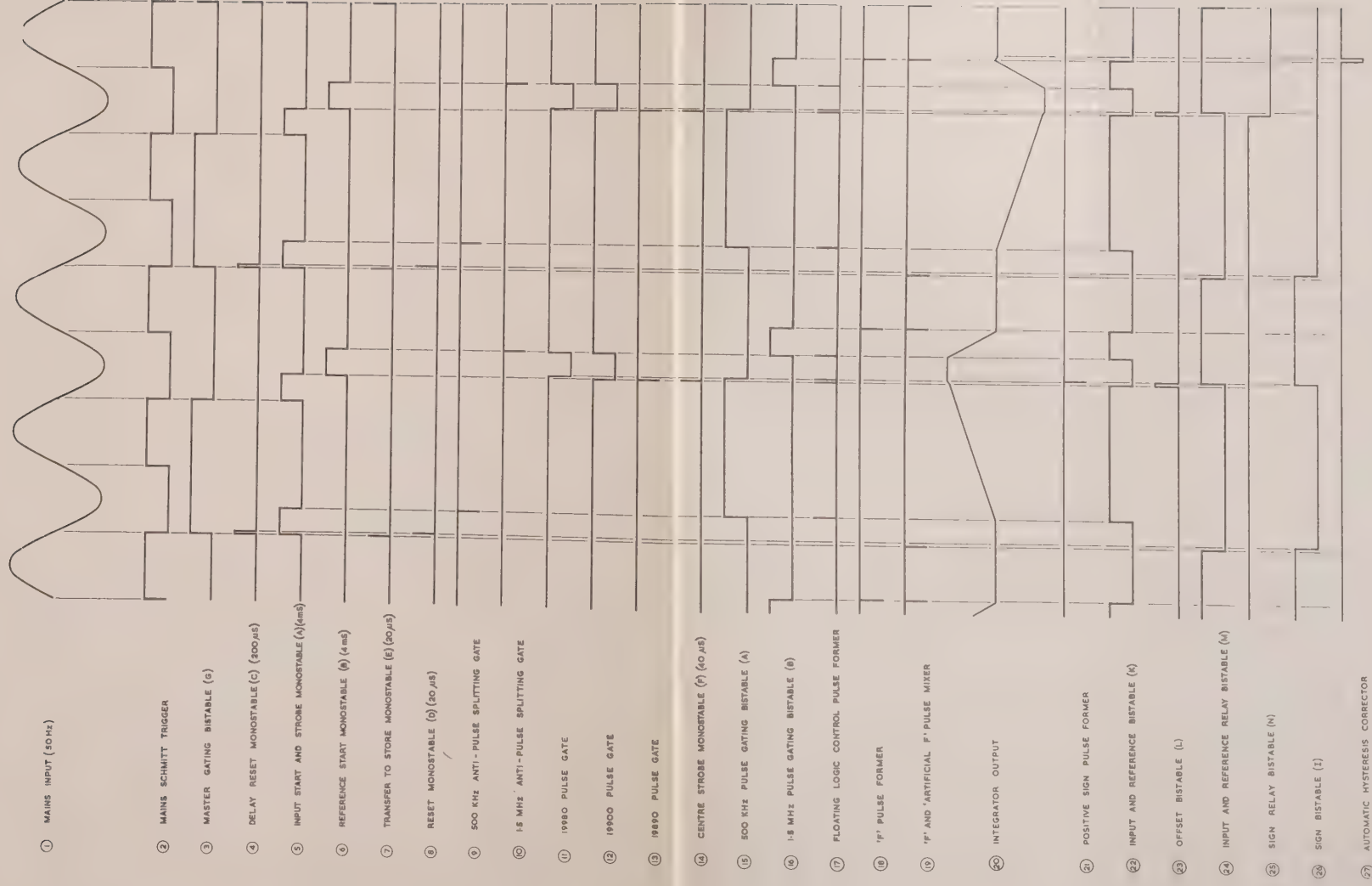


OSCILLATOR CONTROL LOOP TIMING WAVEFORMS

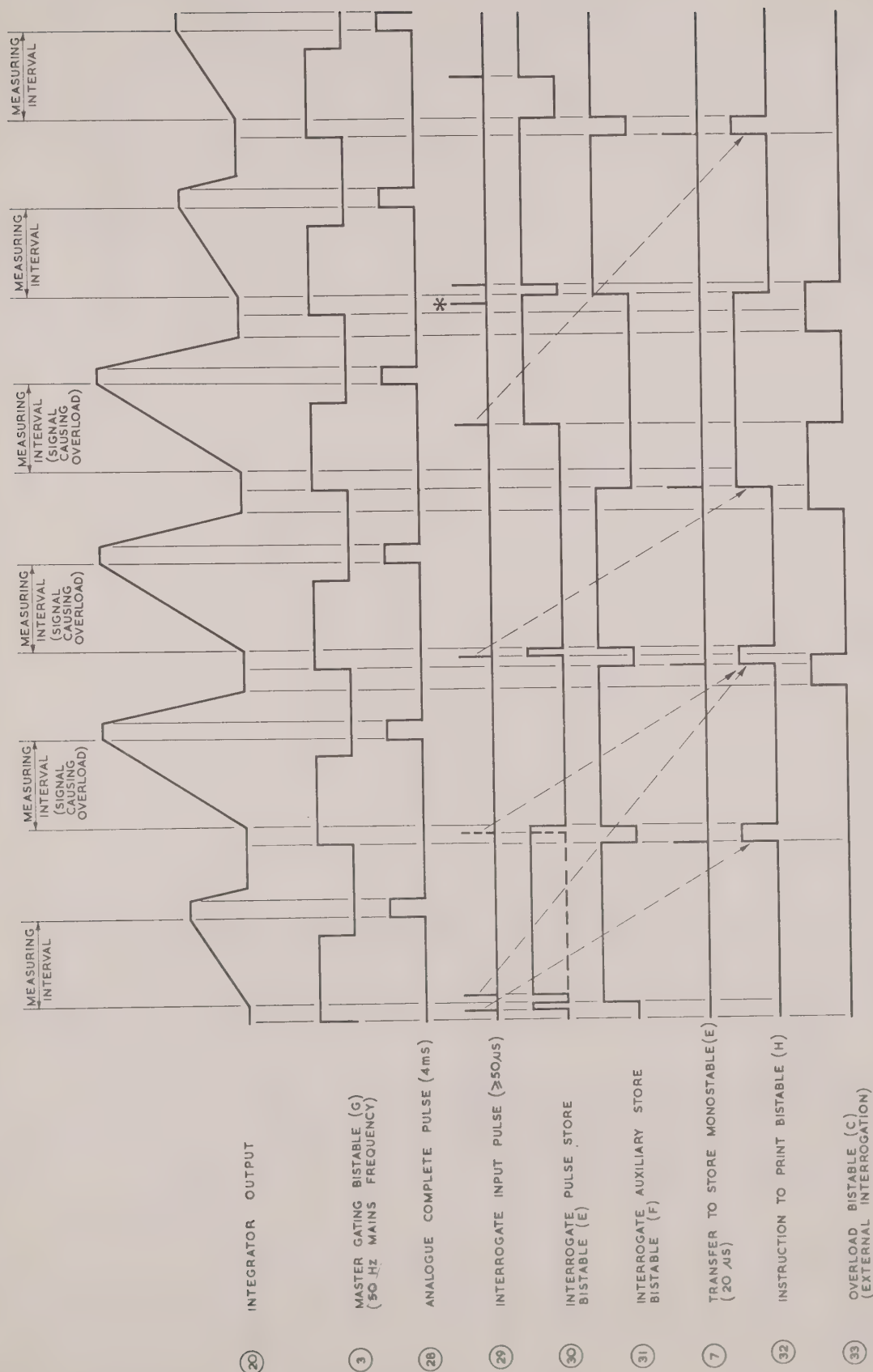


GENERAL BLOCK SCHEMATIC OF OSCILLATOR CONTROL LOOP

FIGURE 7.



MAIN TIMING WAVEFORM DIAGRAM



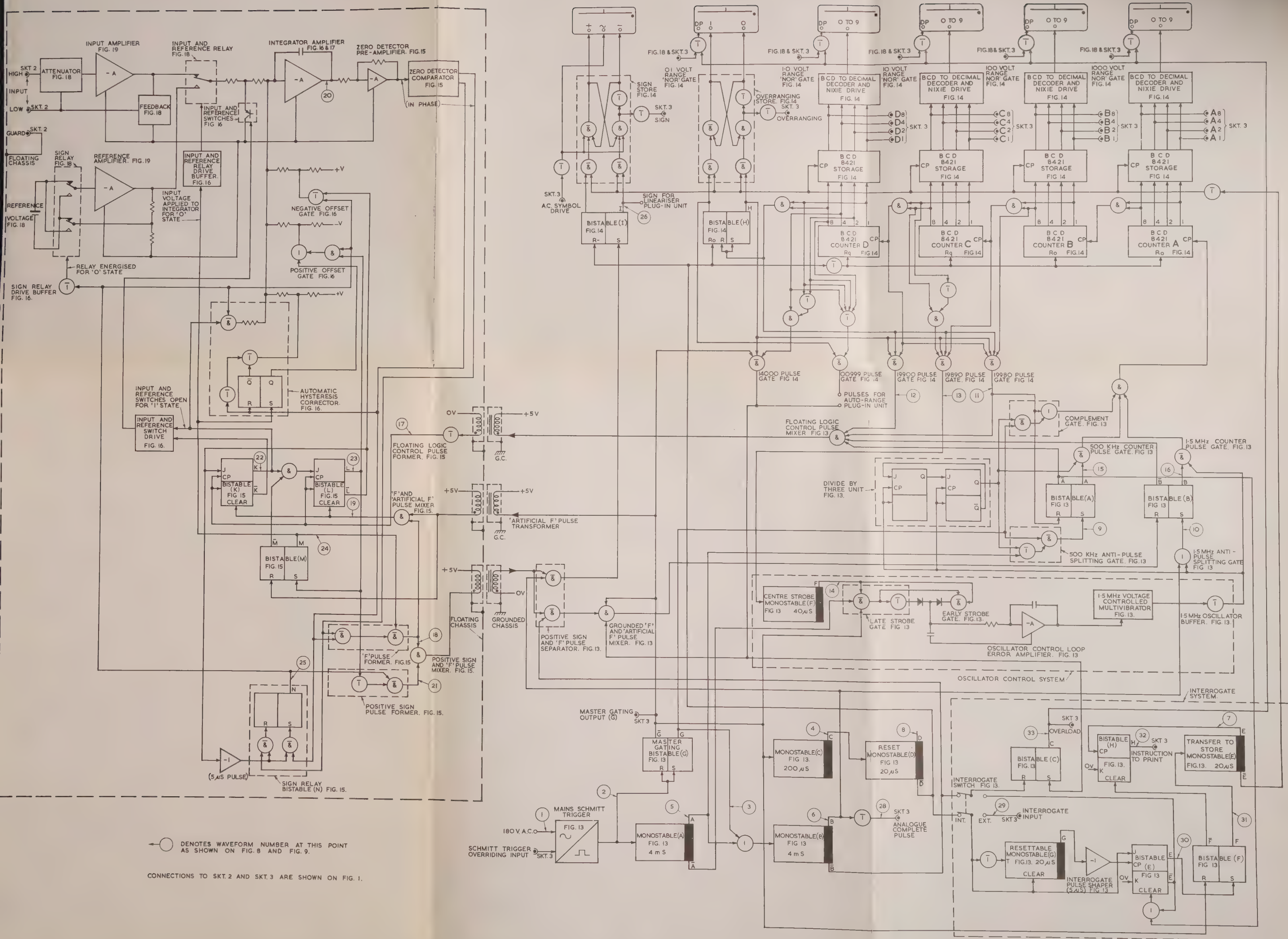
(WAVEFORMS SHOWING THE EFFECT OF INTERROGATION PULSES AT VARIOUS TIMES)

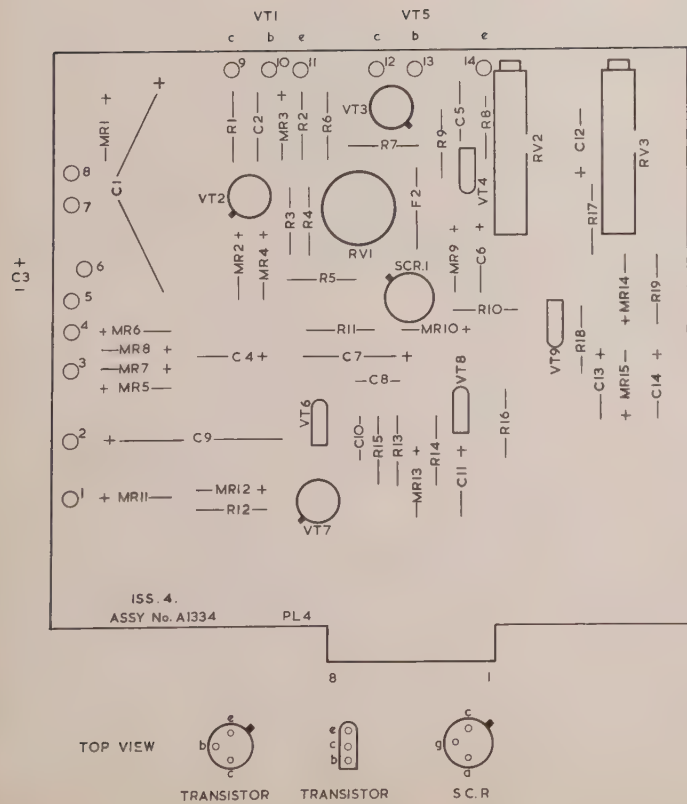
NOTE. WAVEFORM NUMBERS 3, 7 & 20 ARE ALSO SHOWN ON FIG. 8.

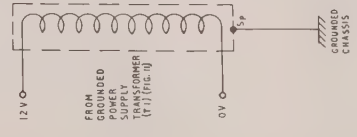
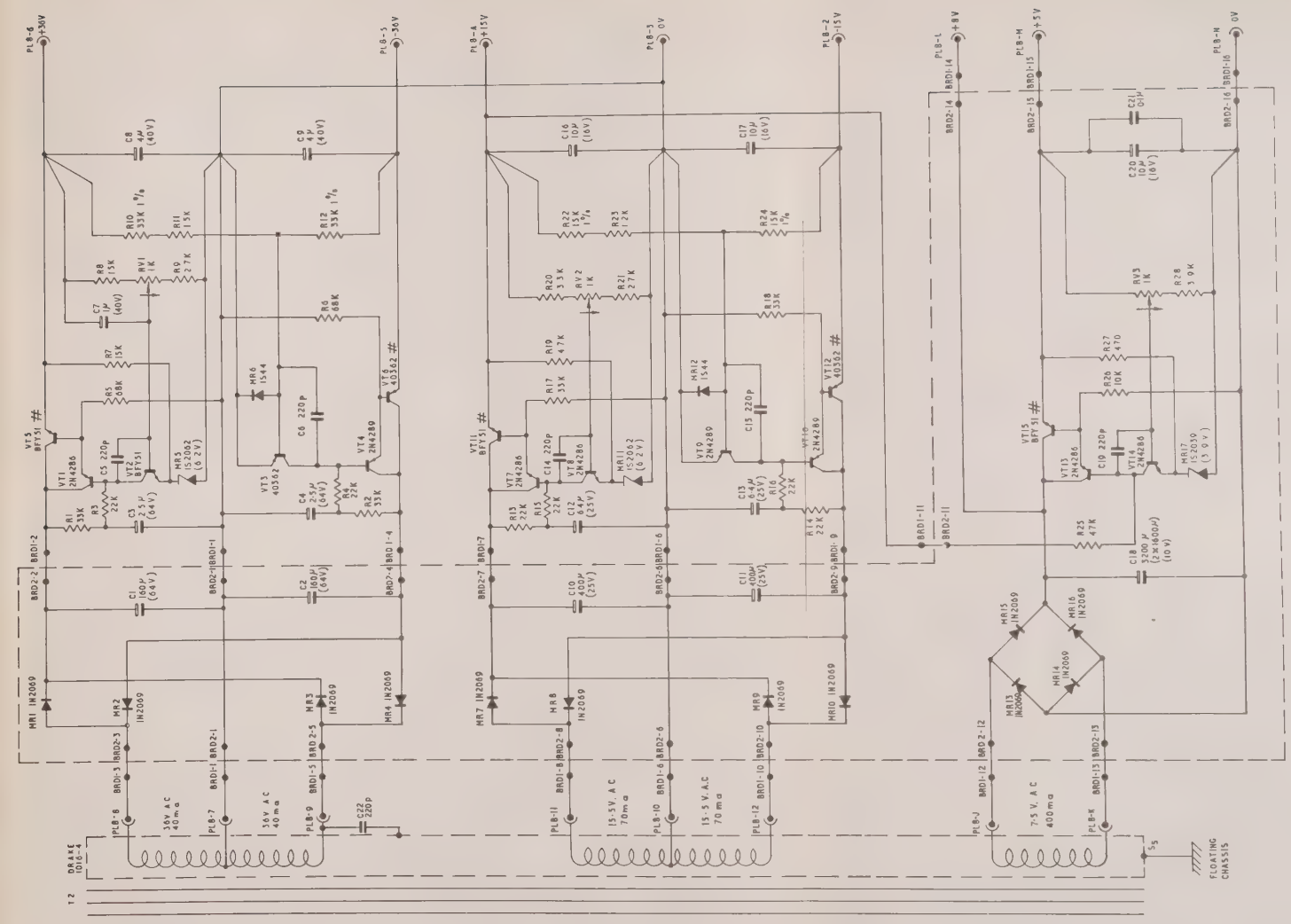
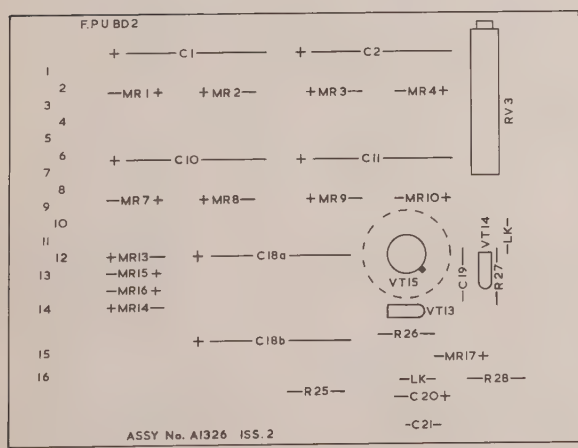
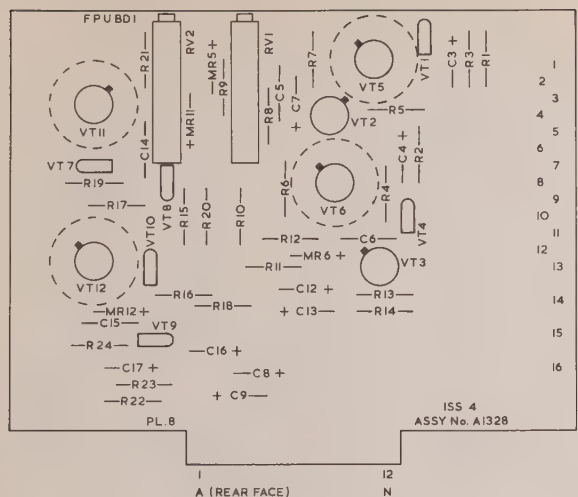
* THIS INTERROGATE PULSE IS NOT ACCEPTED, AS THE INTERROGATE PULSE STORE BISTABLE HAS NOT BEEN RESET.

INTERROGATE SYSTEM TIMING WAVEFORM DIAGRAM

FIGURE 9.

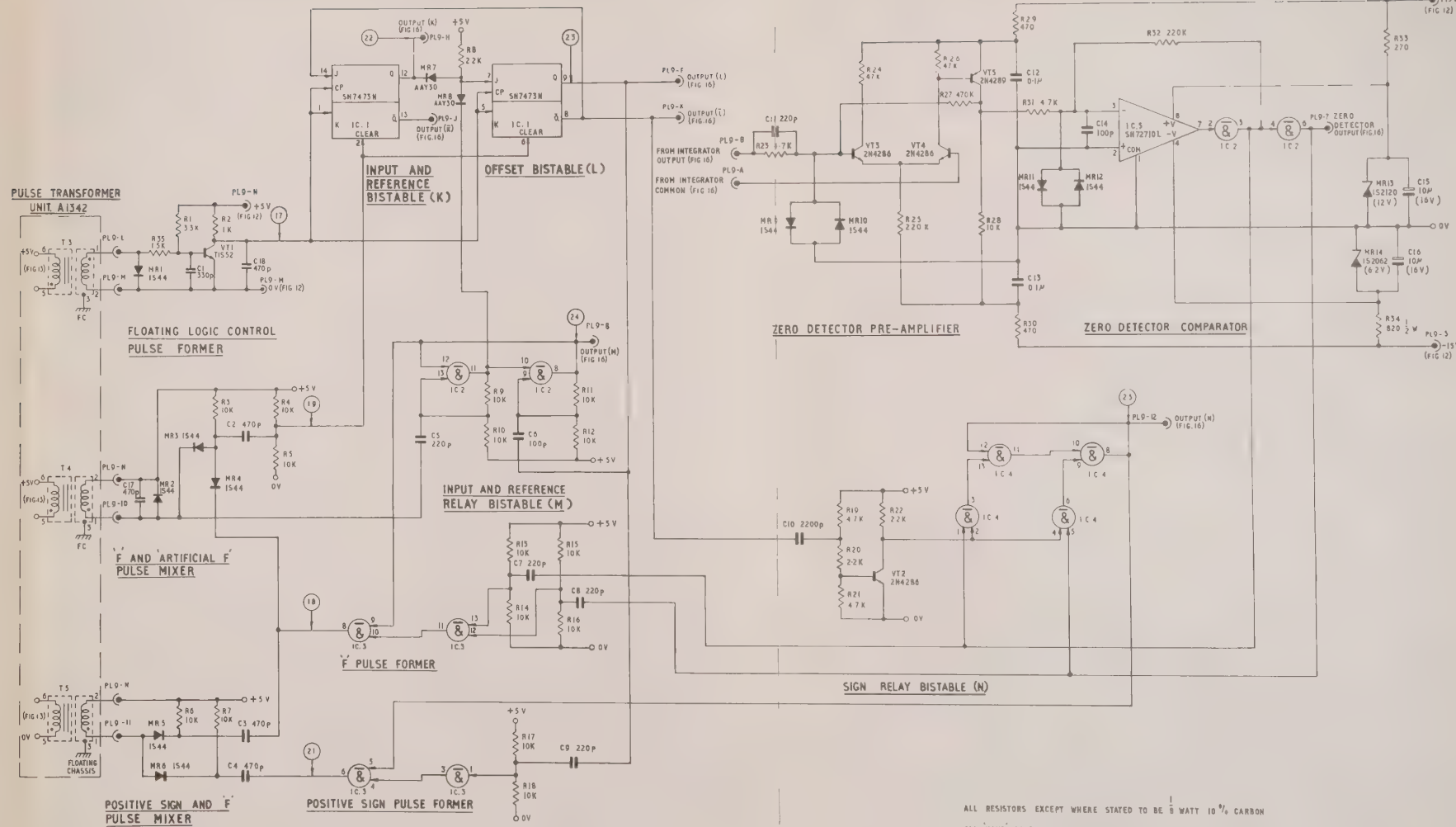
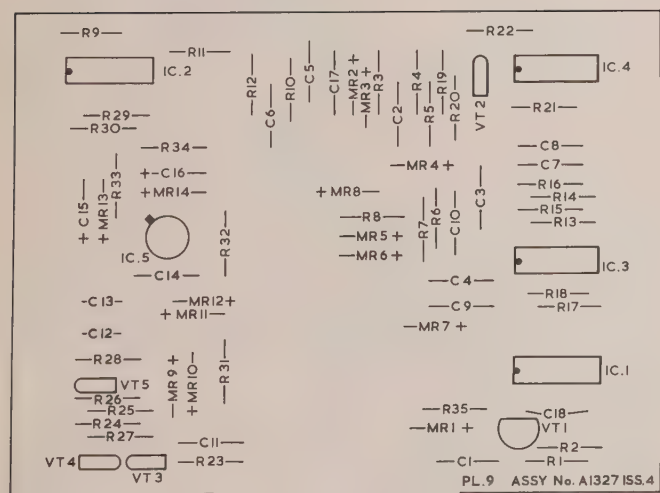






ALL RESISTORS EXCEPT WHERE STATED TO BE 0.1WATT 10% CARBON
 * TRANSISTORS MARKED *HUS REQUIRE HEAT SINKS
 ALTERNATIVE TO 2N4286 IS BC182L1A
 ALTERNATIVE TO 2N4289 IS 2N3702

DVM TYPE 501 FLOATING POWER SUPPLY CIRCUIT DIAGRAM



D V M TYPE 501 FLOATING LOGIC AND ZERO DETECTOR CIRCUIT DIAGRAM

TOP VIEW

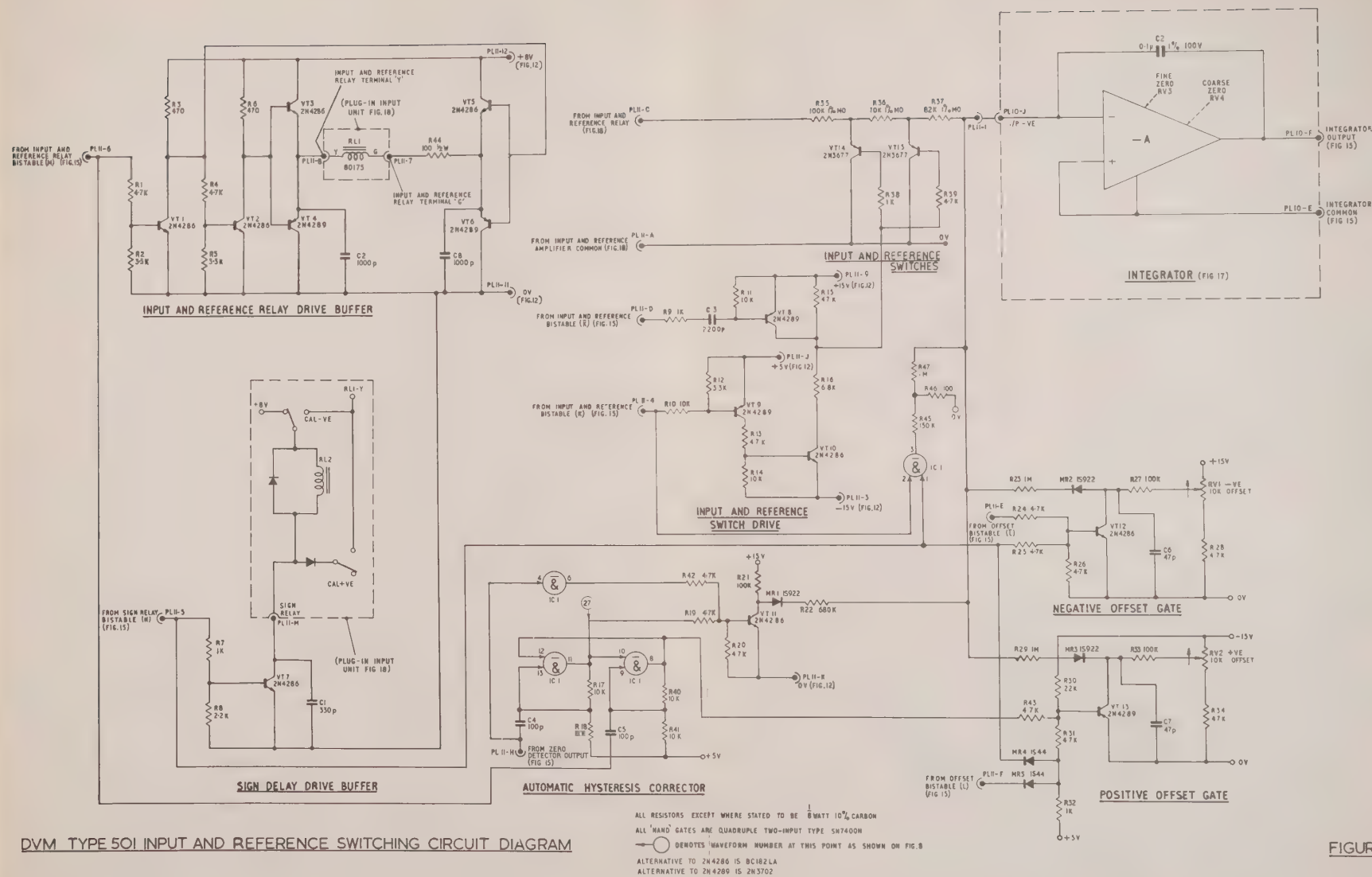
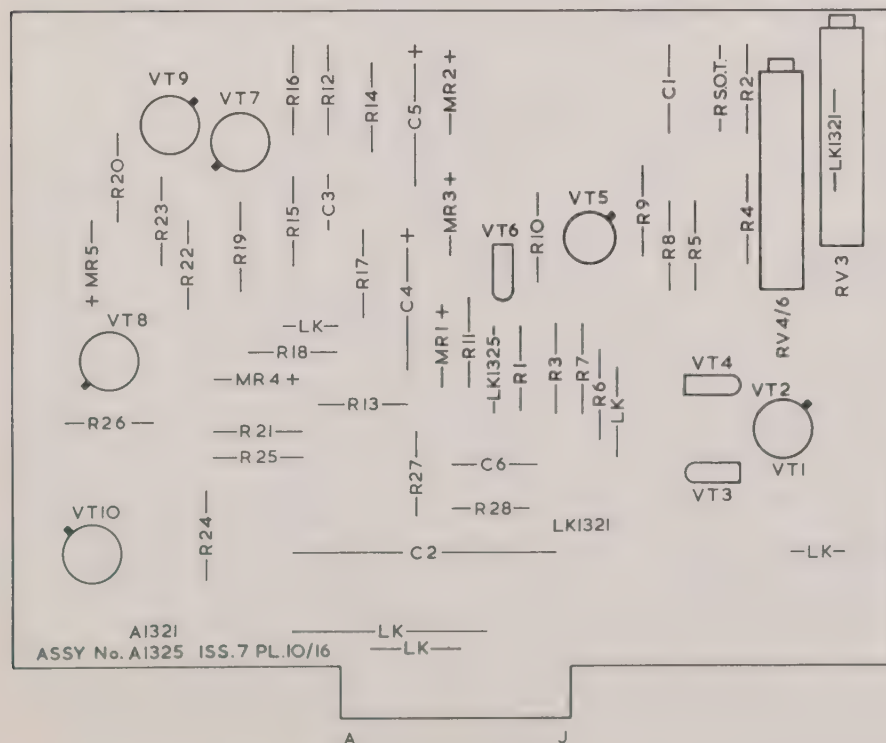
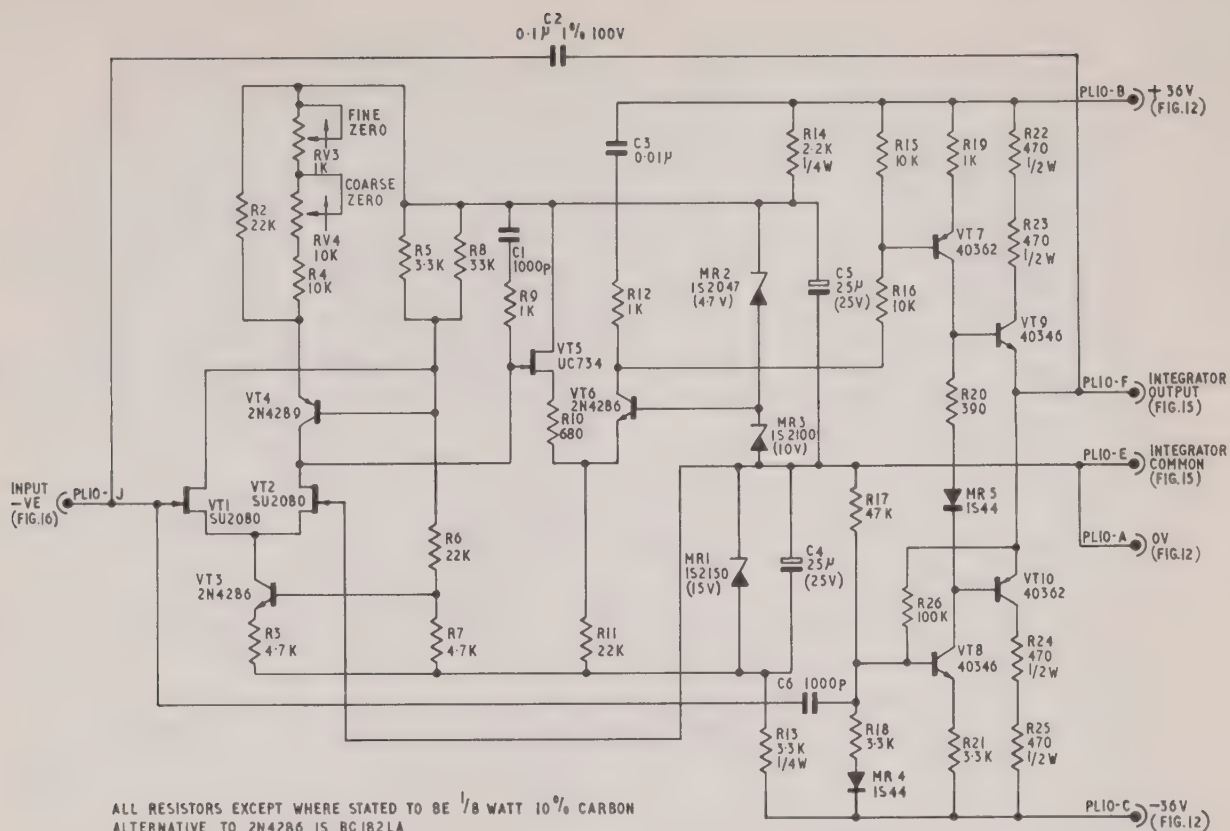


FIGURE 16.



TOP VIEW



Y GN

RV 4

RL 1

RL 2

RL 3

REF. CELL

C2

C3

-LK-

-MRI+

-LK-

-LK-

1 7 6

ISS. 2

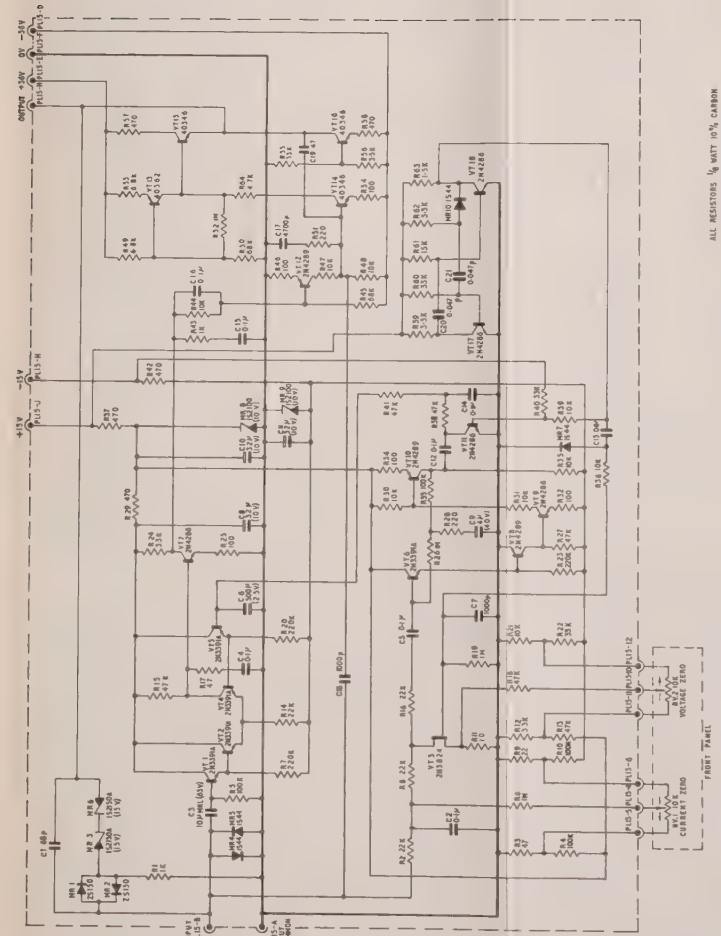
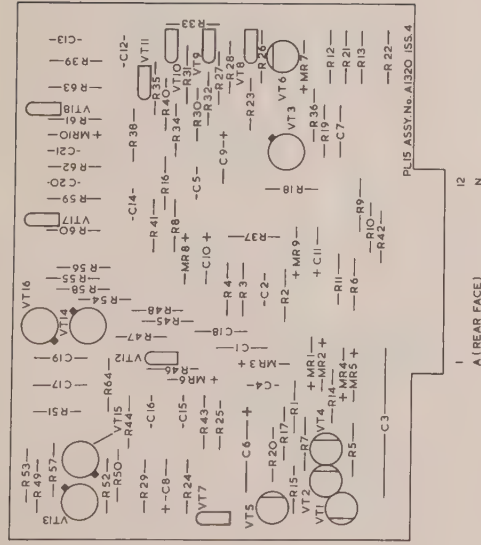
ASSY No. A1322

PL 17

A N



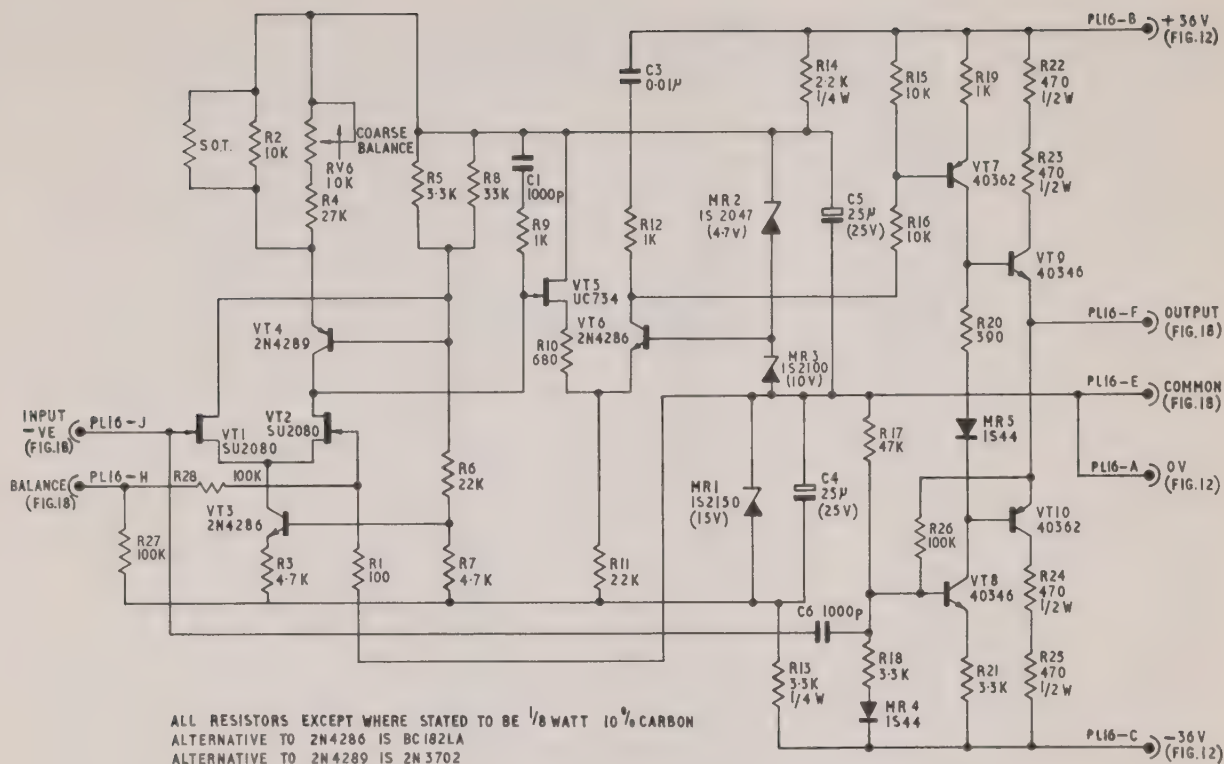
FIGURE 18.



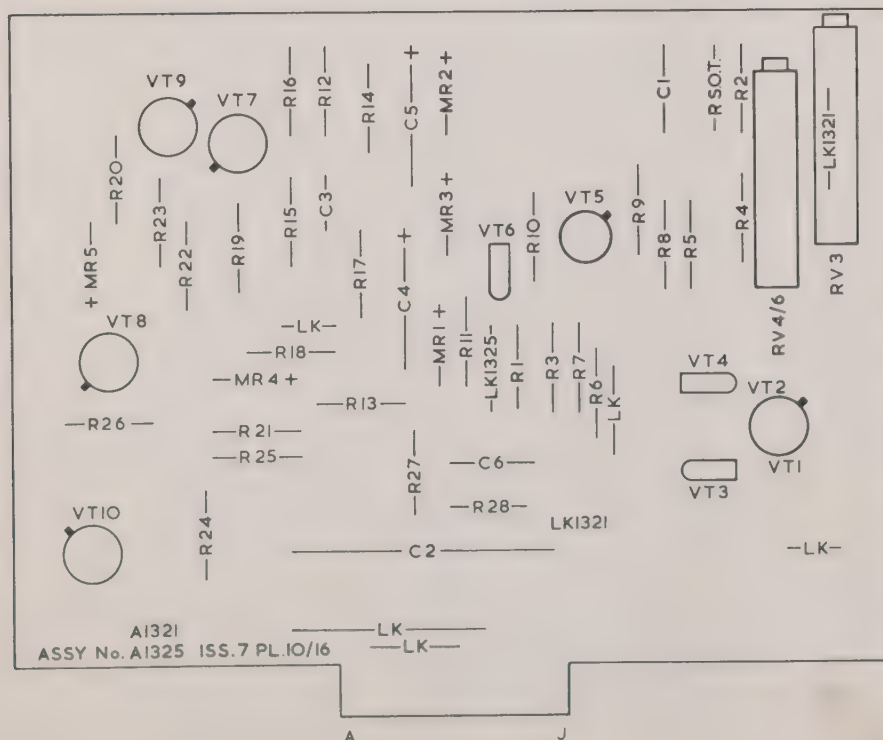
ALL RESISTORS 1/2 WATT 10% CARBON
 ALTERNATIVE TO 2400Ω IS 2.4K
 ALTERNATIVE TO 2400Ω IS 2.4K

FIGURE 19.

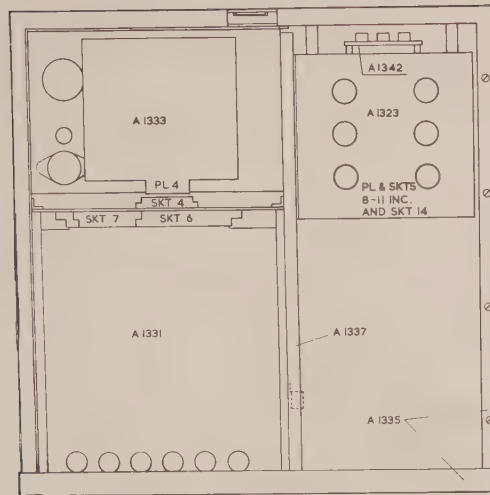
DVM PLUG-IN TYPE A INPUT AMPLIFIER CIRCUIT DIAGRAM



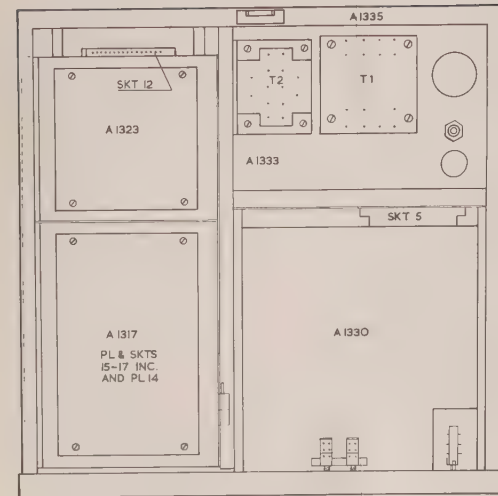
TOP VIEW



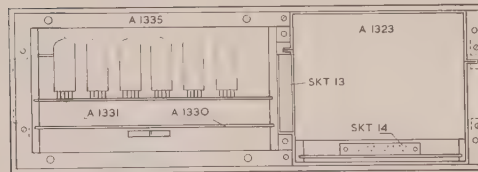
PLAN VIEW



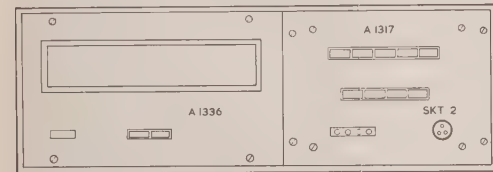
VIEW ON BASE



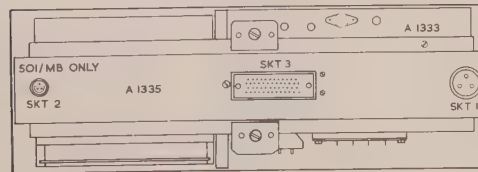
FRONT VIEW WITH PANELS REMOVED



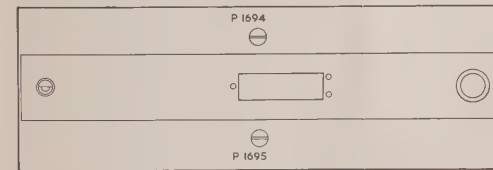
FRONT VIEW WITH PANELS FITTED



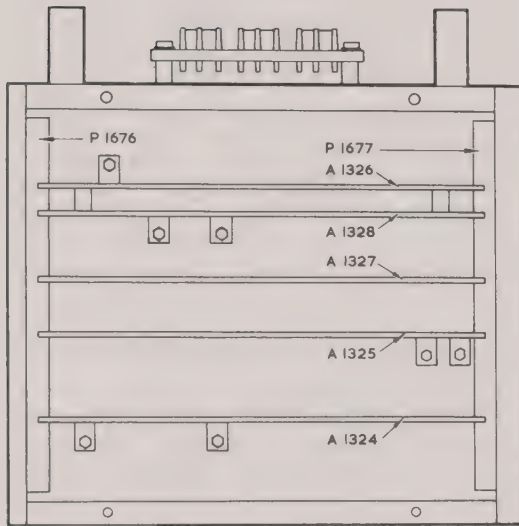
REAR VIEW



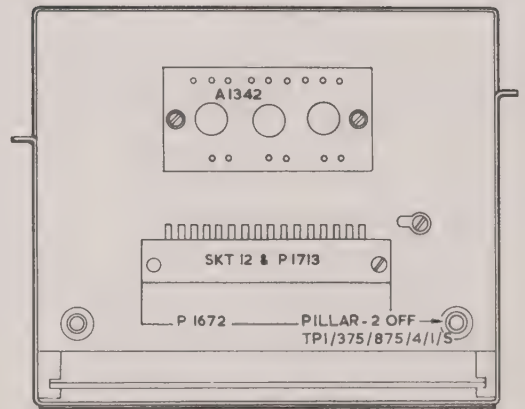
REAR VIEW WITH COVERS FITTED



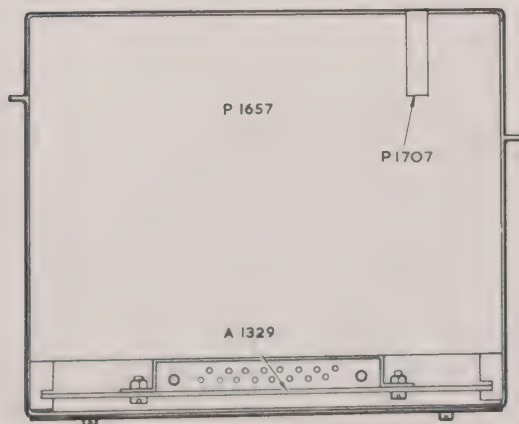
PLAN VIEW



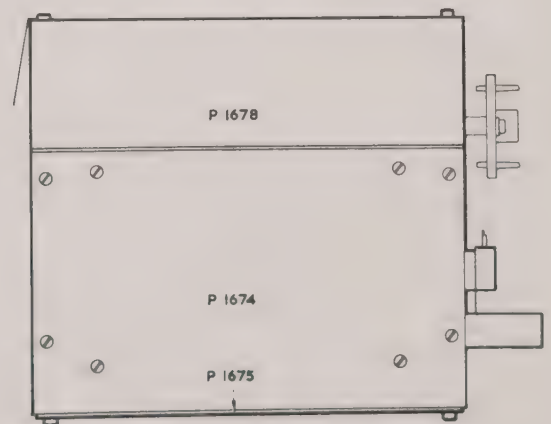
REAR VIEW



FRONT VIEW



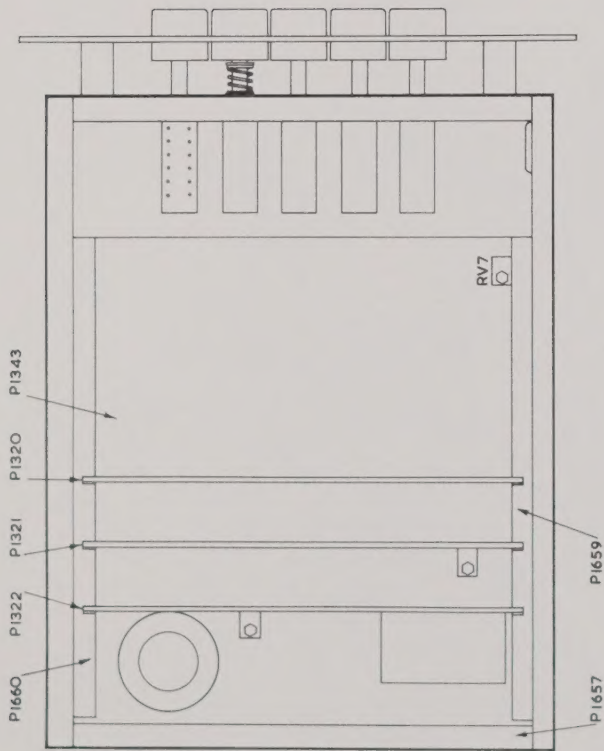
SIDE VIEW



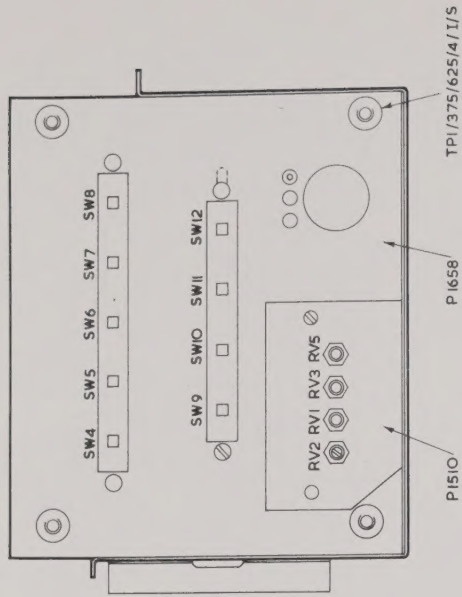
REAR FLOATING UNIT ASSEMBLY (A 1323)

FIGURE 23.

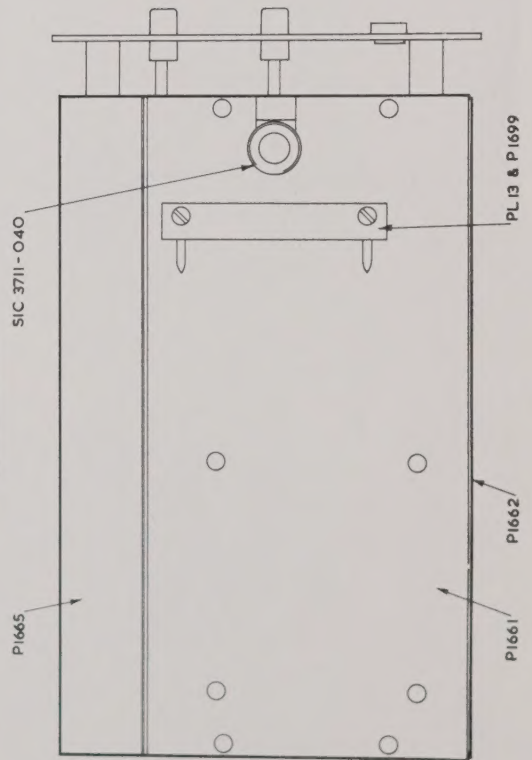
PLAN VIEW



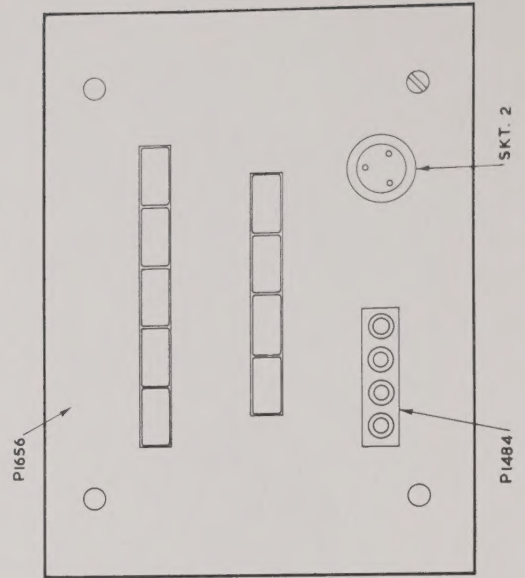
FRONT VIEW WITH FRONT PANEL REMOVED



SIDE VIEW



FRONT VIEW



MP MASTER



MA23403